REALISATION OF AWGN CHANNEL EMULATION MODULES UNDER SISO AND SIMO ENVIRONMENTS FOR 4G LTE SYSTEMS

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ABSTRACT

The testing of a wireless transmitter and receiver in the real-world channel is tedious. So, a channel emulator using FPGA helps in the testing of transmitter and receiver by providing a test environment that simulates a real-world wireless channel. Since FPGAs are flexible, cheap and reconfigurable, they are used in designing an AWGN channel emulator for 4G LTE for Single Input Single Output (SISO) and Single Input Multiple Output (SIMO) environments. In this paper, three basic modules: transmitter, channel estimation and receiver modules are synthesized. In the transmitter module, the input data is 64-QAM modulated and transmitted into the channel. In the channel estimation module, the transmitter data gets multiplied with the channel coefficients and then added with the noise present in the channel. In the receiver module, the data is detected using MMSE estimation. These are implemented in Virtex-5 device using PlanAhead tool and the Resource and Power Estimations are discussed.

KEYWORDS

AWGN, CFI, Channel coefficients, Channel estimation, MMSE, Pre-computed values, QAM modulation.

1. INTRODUCTION

Channel emulators are of great significance in the testing and verification of wireless communication systems. Design and testing of wireless communication systems using simple tools becomes necessary since the present equipment are not accurate and they cost more. Due to the different characteristics of FPGA like, easy integrated mapping, fast processing, low cost and reconfiguration, the synthesis of channel emulation could be done in an effective way.

Long Term Evolution (LTE) of UMTS (Universal Mobile Telecommunication Systems) is a Fourth Generation wireless broadband technology. The main advantages of LTE are high data rate and low latency with reduced cost, when compared with its predecessor GSM.

In this paper, a channel emulator for AWGN (Additive White Gaussian Noise) is designed for SISO and SIMO environments for LTE systems. They are implemented using PlanAhead tool and Virtex-5 device. The channel is estimated on the basis of BER. Bit Error Rate is defined as the ratio of the error bits to the number of bits transmitted. As the Signal-to-noise ratio increases, BER decreases and vice versa.

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2. SYSTEM MODEL

In the transmitter side, it can be observed that the input data is fed into a modulator block. The input data given is four sets of 36 - bits. Those are modulated by means of a 64-QAM modulator. After modulation, the signal is transmitted into the channel, so that it can travel long distances. After modulation, there will be 6 sets of 16 - bit data, sent into the channel.

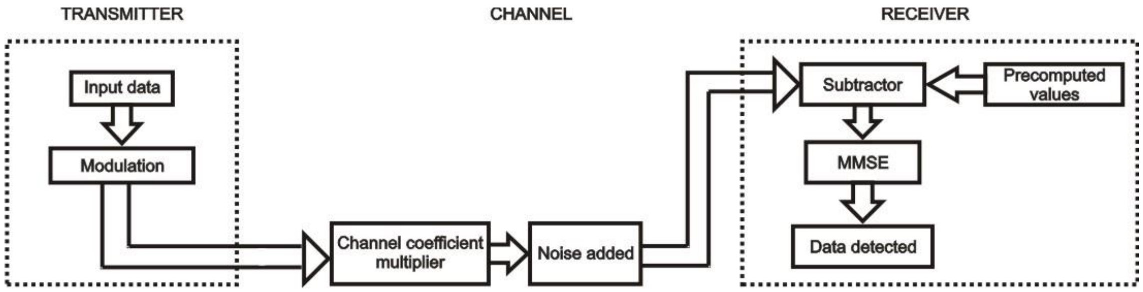


Figure 1. System Model of Channel Emulation process

In the channel, the 6 sets of 16 - bit modulated data are multiplied with the16 sets of 16 - bit channel coefficients which are already present in the channel. Then the resulting data will be added with the noise present in the channel. Channel coefficients are the discrete-time impulse response of the channel. Ideally, one transmitting symbol gives an output only in one symbol time without interfering with other symbols. The 16 sets of 16 - bit data which are already present in the channel are of random in nature. These values are not directly added with the multiplied values. Instead, the 6 sets of 16 - bit noise are multiplied with the variance.

The formula for variance is given by,

$$\text{Variance}= 1 \ \ \text{sqrt} \ \ 2 \ \ * \ \ 10^{\wedge} \ \text{-SNR} \ \ 20 \qquad \ldots\ldots.(1)$$

The noise value after getting multiplied with the variance gets added with the multiplied values. This value is received by the receiver.

In the receiver side, the data from the channel is received and it is subtracted from a set of pre-computed values. The pre-computed values are the product of the 6 sets of 16 - bit QAM modulated signal with the 6 sets of 16 - bit channel coefficients. It does not contain the noise which is present in the channel. After subtraction, the resultant value is given as input to the Minimum Mean Square Error estimator (MMSE), to find the minimum value. That minimum value is called as Control Format Indicator (CFI). The data corresponding to the CFI is given as the output by the receiver. The input data is a complex one and hence the output will also be a complex one.

The complex-valued output at the k-th receiving antenna is modelled as,

$$y_k = h_k \circ d(n) + u_k, \quad k = 1, 2, ...K \qquad \ldots\ldots..(2)$$

where, y is the received signal, h is the channel coefficient and u is the noise.
The minimum value will be calculated by,

$$\mathrm{CFI} = \min_{m=1,2,3} \ {}_{k=1}^{K} y_k - \ h_k \circ d^{\,m} \quad {}^{2} \qquad \text{……..(3)}$$

which simplifies to

$$\mathrm{CFI} = \arg_{m=1,2,3} z^{(m)} \qquad \text{……..(4)}$$

where the soft outputs are given by,

$$z^{\,m} = \ {}_{k=1}^{K} z_k^{\,m} \quad \text{for } m = 1,2,3 \qquad \text{……..(5)}$$

where $z_k^{\,m} = \mathrm{Re} \ \ y_k \circ h_k^{*}, d^{\,m}$ for $m = 1,2,3$.

By means of these equations [1], the minimum CFI value is calculated. Then the output retrieved by the receiver is compared with the original data. For every correct value, a counter will count the values. Based on this, BER graph is drawn.

In the case of SISO, there will be a single receiving antenna, whereas in the case of SIMO, there will be two receiving antennae.

3. Architecture of SISO

The architecture of SISO consists of only one transmitting antenna and one receiving antenna as shown in Figure 2.

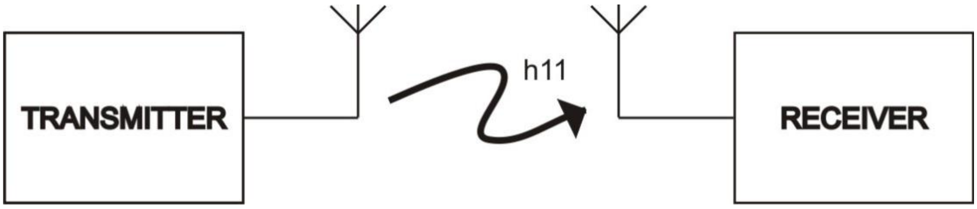


Figure 2. Basic block diagram of SISO

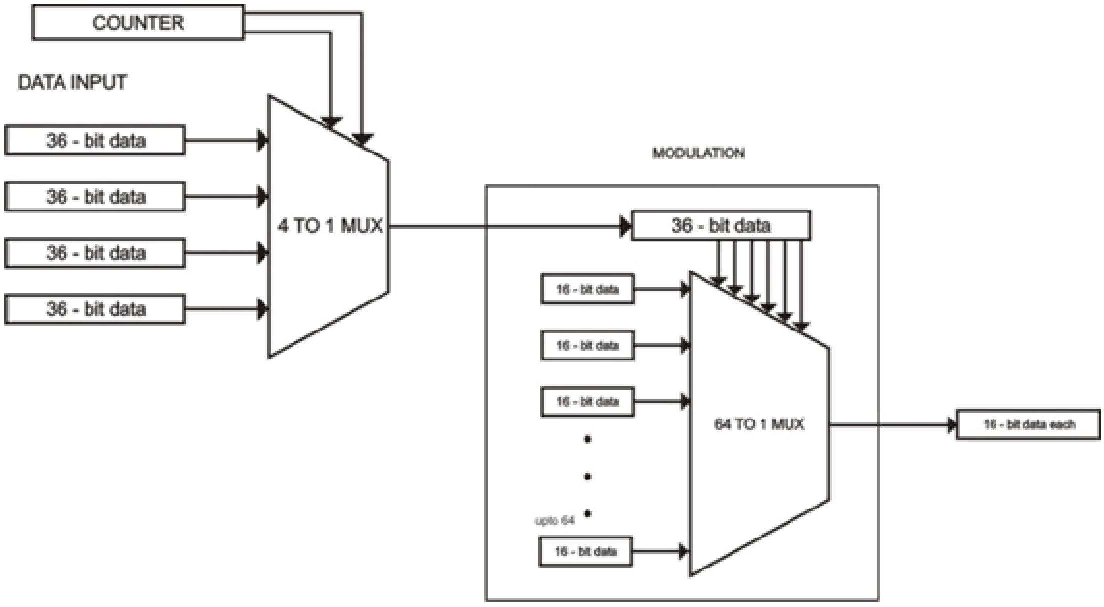


Figure 3. Transmitter side architecture of SISO

From the Figure 3, it is observed that the input given is four sets of 36 - bit data (18 - bit real, 18 - bit imaginary). The output data are given as input to a 4 to 1 MUX. The 2 - bit control input to the MUX are given by a 2 - bit counter. The counter will count for every clock cycle. So for every clock pulse a 36 - bit data will be sent out of the MUX. The next block is a 64-QAM Modulator block. The QAM modulator block consists of four sets of 16 - bit given as input to a 4 to 1 MUX. Each 2 - bit data from the received 36 - bit will act as the control input to the MUX. This is performed by means of a 2 - bit shifter. Based on the values of the 2 - bit data, a 16 - bit data will be given as the output from the modulator. The output will be the QAM modulated signal. Since from a 36 - bit data, modulation takes place for every 2 - bits, the output will be 6 sets of 16 - bit QAM modulated signal. Thus for every clock pulse the output will be 6 sets of 16 - bit QAM modulated signal.

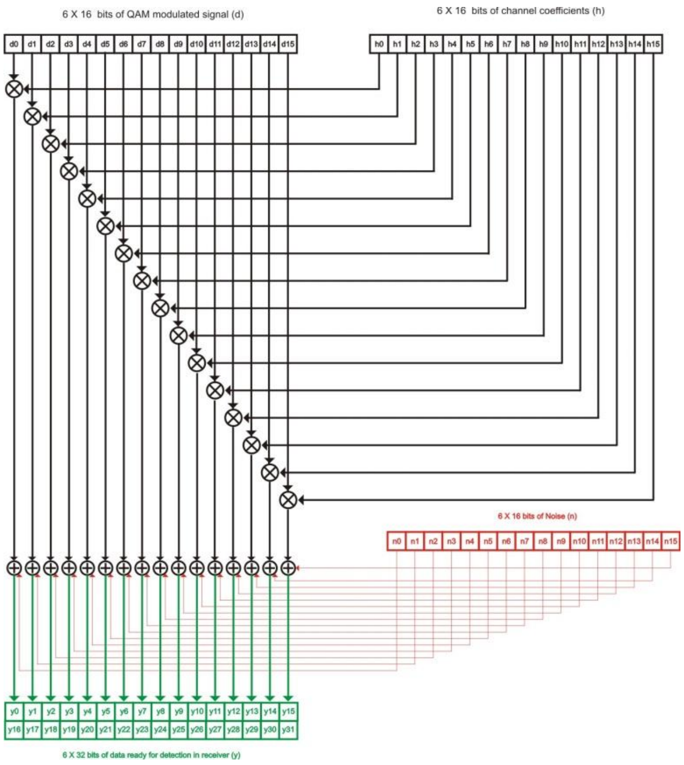

6 X 16 bits of QAM modulated signal (d)
d0 d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11 d12 d13 d14 d15
6 X 16 bits of channel coefficients (h)
h0 h1 h2 h3 h4 h5 h6 h7 h8 h9 h10 h11 h12 h13 h14 h15
6 X 16 bits of Noise (n)
n0 n1 n2 n3 n4 n5 n6 n7 n8 n9 n10 n11 n12 n13 n14 n15
y0 y1 y2 y3 y4 y5 y6 y7 y8 y9 y10 y11 y12 y13 y14 y15
y16 y17 y18 y19 y20 y21 y22 y23 y24 y25 y26 y27 y28 y29 y30 y31
6 X 32 bits of data ready for detection in receiver (y)

Figure 4. Channel Estimation architecture of SISO

From the Figure 4, it is can be seen that the output from the transmitter side, which is the 6×16 bits QAM modulated signal, is multiplied with the 6×16 bits of channel coefficients [5]. Then the multiplied value is added with the 6×16 bits of noise which is present in the channel. The noise which gets added will be a product of the variance and the noise. The resulting output will be 6×32 bits of data which is to be received by the receiver.

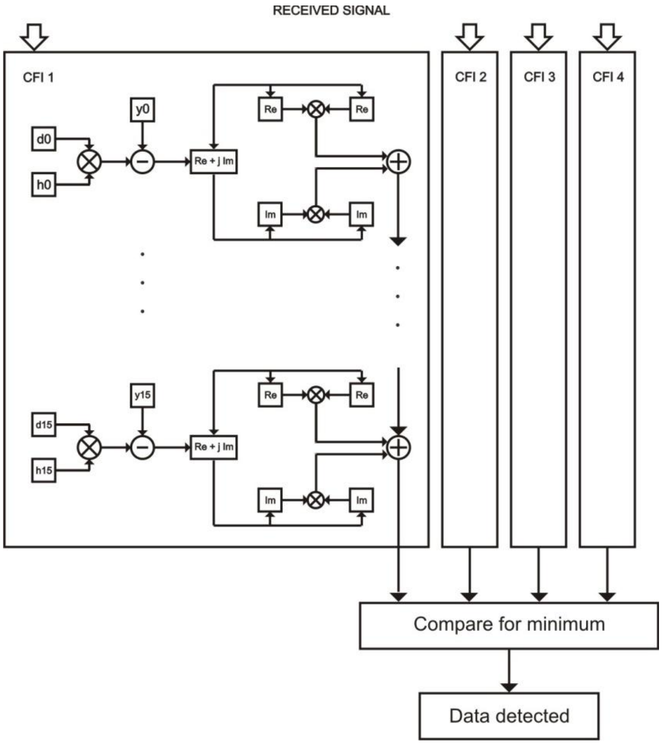


Figure 5. Receiver side architecture of SISO

From the Figure 5, it is observed that in the receiver side, pre-computed data will be present. The pre-computed data is the product of the QAM modulated signal and the channel coefficients value. From the received data, the pre-computed values are subtracted. From the obtained result, real parts and imaginary parts are separately squared and added with each other. This is performed for all the 6 sets of 16 bit data. This is for a single clock pulse. Similarly for all the clock cycles, the values are calculated. Since there are four sets of 36 - bit data, after four clock cycles only the output can be obtained [6]. Hence there will be a delay of four clock cycles. After four clock cycles, there will be four sets of values. These values are compared for minimum, by means of Minimum Mean Square Error (MMSE) estimator algorithm. From this, the minimum value is detected and it is given as the detected output.

4. ARCHITECTURE OF SIMO

The architecture of SIMO consists of only one transmitting antenna and many receiving antennae. In this paper, a 1×2 SIMO is considered (i.e.) one transmitting antenna and two receiving antennae, as shown in Figure 6.

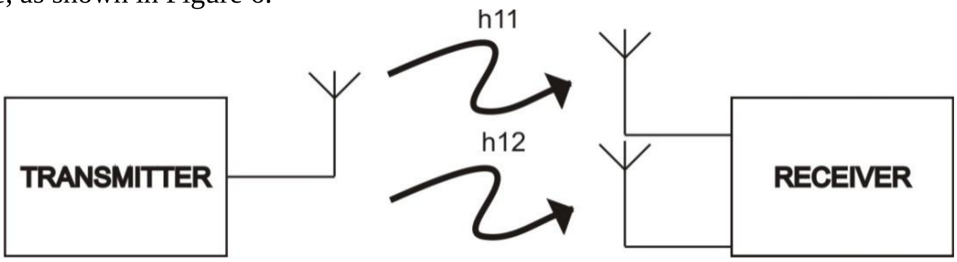
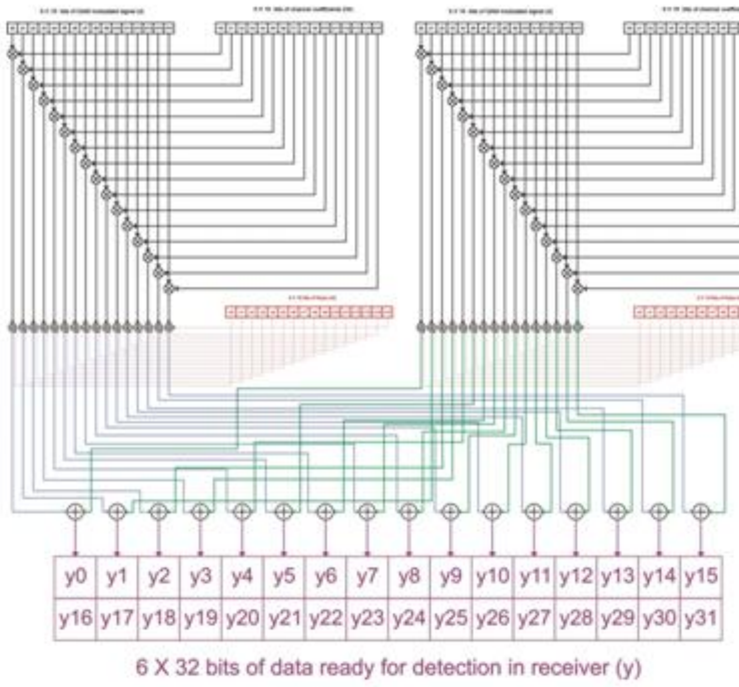


Figure 6. Basic block diagram of SIMO

The transmitter block of SIMO is similar to that of SISO. But the channel estimation and receiver blocks will vary.



y0	y1	y2	y3	y4	y5	y6	y7	y8	y9	y10	y11	y12	y13	y14	y15
y16	y17	y18	y19	y20	y21	y22	y23	y24	y25	y26	y27	y28	y29	y30	y31

Figure 7. Channel Estimation architecture of SIMO

From the Figure 7, it is observed that the output from the transmitter side, which is the 6×16 bits QAM modulated signal, is multiplied with two sets of 6×16 bits of channel coefficients, which are h0 and h1. After that, there will be two sets of multiplied values. These values are added with two sets 6×16 bits of noise, which are n0 and n1, which is present in the channel. The noise which gets added will be a product of the variance and the noise. Then the two sets of values are added with each other. The resulting output will be 6×16 bits of data which is to be received by the receiver [5].

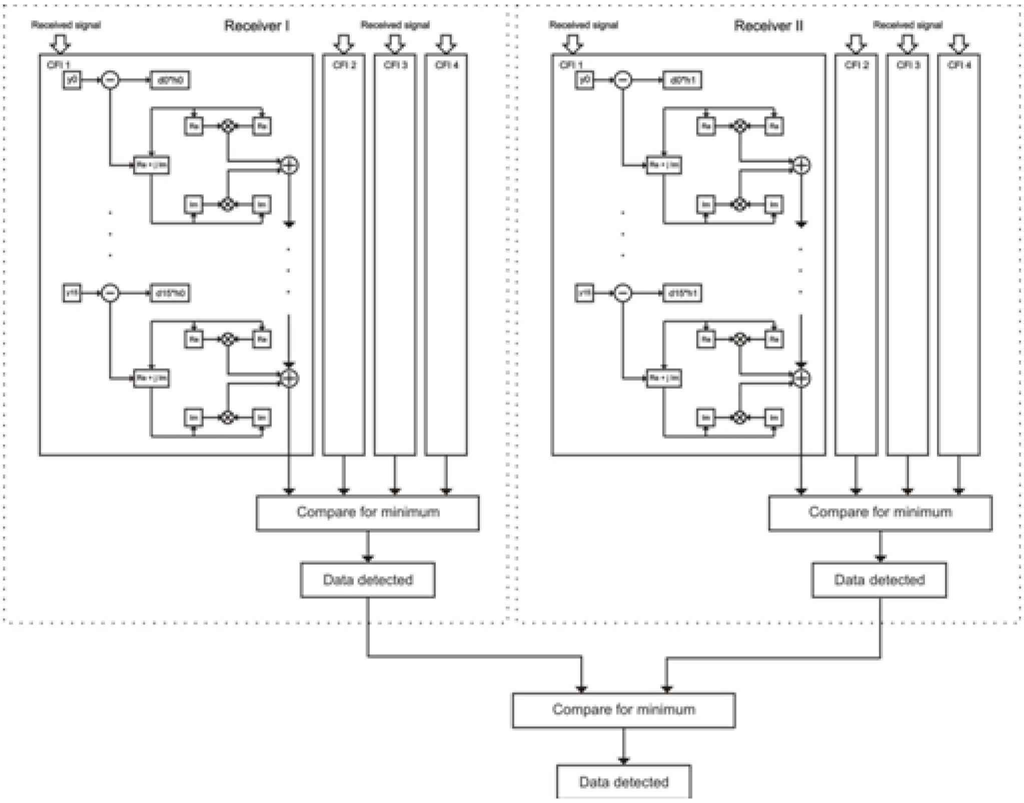


Figure 8. Receiver side architecture of SIMO

In general, in the receiver side, pre-computed data will be present. In the Figure 8, there are two receivers. So, Receiver I will contain pre-computed data which is the product of the QAM modulated signal and the channel coefficients value of h0. In Receiver II, the pre-computed data is the product of the QAM modulated signal and the channel coefficients value of h1. But in both the receivers, the received data will be the same [6].

In each receiver, from the received data, the pre-computed values are subtracted. From the obtained result, real parts and imaginary parts are separately squared and added with each other. This is performed for all the 6 sets of 16 bit data. This is for a single clock pulse. Similarly for all the clock cycles, the values are calculated. Since there are four sets of 36 - bit data, after four clock cycles only the output can be obtained. Hence there will be a delay of four clock cycles.

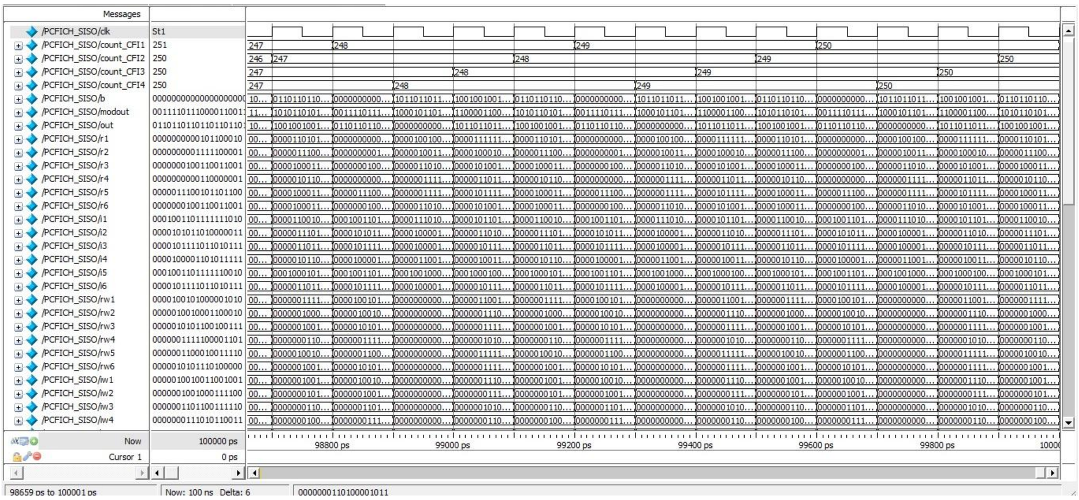
After four clock cycles, there will be four sets of values, the values of CFI. These values are compared for minimum, by means of Minimum Mean Square Error (MMSE) estimator algorithm. From this, the minimum value is detected and it is given as the detected output. All these processes are executed separately for both the receivers. Finally from the detected output value from both the receivers, the minimum value is calculated. That value is considered as the original data, which is transmitted by the transmitter.

5. RESULTS AND DISCUSSIONS

Simulation is performed in Modelsim and implementation is accomplished by PlanAhead tool in Virtex-5 device.

5.1. Simulation Result

5.1.1. SISO



Messages	
/PCFICH_SISO/clk	St1
/PCFICH_SISO/count_CFI1	251
/PCFICH_SISO/count_CFI2	250
/PCFICH_SISO/count_CFI3	250
/PCFICH_SISO/count_CFI4	250
/PCFICH_SISO/b	0000000000000000000
/PCFICH_SISO/modout	0011110111000011001
/PCFICH_SISO/out	0110110110110110110
/PCFICH_SISO/r1	000000000101100010
/PCFICH_SISO/r2	000000001111100001
/PCFICH_SISO/r3	000000100110011001
/PCFICH_SISO/r4	000000000110000001
/PCFICH_SISO/r5	0000011100101101100
/PCFICH_SISO/r6	000000100110011001
/PCFICH_SISO/i1	000100110111111010
/PCFICH_SISO/i2	000010101101000011
/PCFICH_SISO/i3	0000101111011010111
/PCFICH_SISO/i4	0000100001101011111
/PCFICH_SISO/i5	000100110111110010
/PCFICH_SISO/i6	0000101111011010111
/PCFICH_SISO/rw1	0000100101000001010
/PCFICH_SISO/rw2	0000010010001100010
/PCFICH_SISO/rw3	0000010101100100111
/PCFICH_SISO/rw4	0000001111100001101
/PCFICH_SISO/rw5	0000001100010011110
/PCFICH_SISO/rw6	0000010101110100000
/PCFICH_SISO/iw1	0000010010011001001
/PCFICH_SISO/iw2	0000001001000111100
/PCFICH_SISO/iw3	0000001101100111110
/PCFICH_SISO/iw4	0000000111010110011
Now	100000 ps
Cursor 1	0 ps

98659 ps to 100001 ps

Now: 100 ns Delta: 6

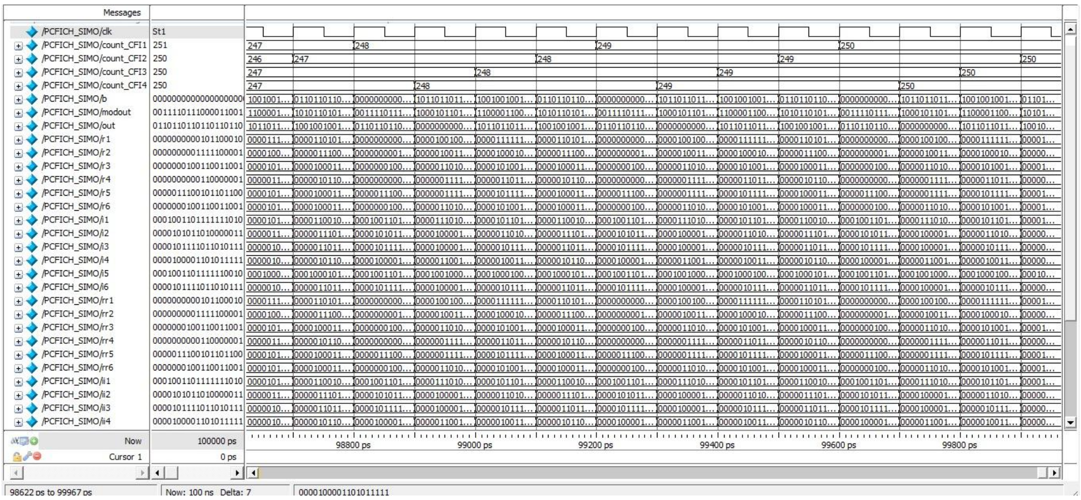
0000000110100001011

Figure 9. Simulation Result of SISO

From the Figure 9, it is observed that “clk” (clock) is the input given. The outputs count_CFI 1, count_CFI 2, count_CFI 3,count_CFI 4 are the count values which indicate the number of times the original data retrieved at the receiver is equal to the input data given. The Figure 9 indicates the simulation result for a case with variance 0. If the value of variance is 0, then there will be no noise and hence it is the ideal case. So there will be perfect reception of the transmitted signal at the receiver side. However, there will be a delay of four clock pulses and hence each output is counted after four clock pulses. So in the above case, for an input of 1000 clock pulses, the four sets of 36 - bit input data are retrieved 250 times in the Receiver.

5.1.2. SIMO

From the Figure 10, it is observed that “clk” (clock) is the input given. The outputs count1_CFI 1, count1_CFI 2, count1_CFI 3, count1_CFI 4 are the count values which indicate the number of times the original data is retrieved at the receiving end in Receiver I is equal to the input data given in the transmitting end. Similarly, the outputs count2_CFI 1, count2_CFI2, count2_CFI3, count2_CFI4 are the count values which indicate the number of times the original data retrieved at the receiving end in Receiver II is equal to the input data given in the transmitting end.



```
Messages
/PCFICH_SIMO/clk          St1
/PCFICH_SIMO/count_CFI1   251
/PCFICH_SIMO/count_CFI2   250
/PCFICH_SIMO/count_CFI3   250
/PCFICH_SIMO/count_CFI4   250
/PCFICH_SIMO/b            0000000000000000000
/PCFICH_SIMO/modout       001111011100001100 1
/PCFICH_SIMO/out          0110110110110110110
/PCFICH_SIMO/r1           0000000000101100010
/PCFICH_SIMO/r2           0000000001111100001
/PCFICH_SIMO/r3           0000000100110011001
/PCFICH_SIMO/r4           0000000000110000001
/PCFICH_SIMO/r5           0000011100101101100
/PCFICH_SIMO/r6           0000000100110011001
/PCFICH_SIMO/i1           0001001101111111010
/PCFICH_SIMO/i2           0000101011010000011
/PCFICH_SIMO/i3           0000101111011010111
/PCFICH_SIMO/i4           0000100001101011111
/PCFICH_SIMO/i5           0001001101111110010
/PCFICH_SIMO/i6           0000101111011010111
/PCFICH_SIMO/rr1          0000000000101100010
/PCFICH_SIMO/rr2          0000000001111100001
/PCFICH_SIMO/rr3          0000000100110011001
/PCFICH_SIMO/rr4          0000000000110000001
/PCFICH_SIMO/rr5          0000011100101101100
/PCFICH_SIMO/rr6          0000000100110011001
/PCFICH_SIMO/ii1          0001001101111111010
/PCFICH_SIMO/ii2          0000101011010000011
/PCFICH_SIMO/ii3          0000101111011010111
/PCFICH_SIMO/ii4          0000100001101011111
Now                       100000 ps
Cursor 1                  0 ps
98622 ps to 99967 ps      Now: 100 ns  Delta: 7      0000100001101011111
```

Figure 10. Simulation Result of SIMO

The Figure 10 indicates the simulation result for a case with variance 0. If the value of variance is 0, then there will be no noise and hence it is the ideal case. So there will be perfect reception of the transmitted signal at the receiver side. However, there will be a delay of four clock pulses and hence each output is counted after four clock pulses. So in the above case, for an input of 1000 clock pulses, the four sets of 36 - bit input data are retrieved 250 times in both the Receiver I and Receiver II.

5.2. FPGA Editor

In the FPGA Editor, the programmable elements are called Configurable Logic Blocks (CLB). A CLB contains LUTs (Look Up Table) and (Flip Flops) FFs/Latches. The LUTs and FFs are organized in Slices.

5.2.1. SISO

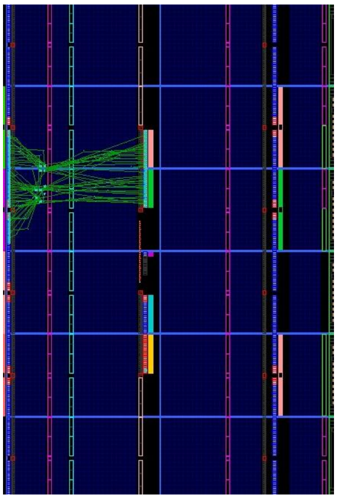


Figure 11. FPGA Editor of Transmitter

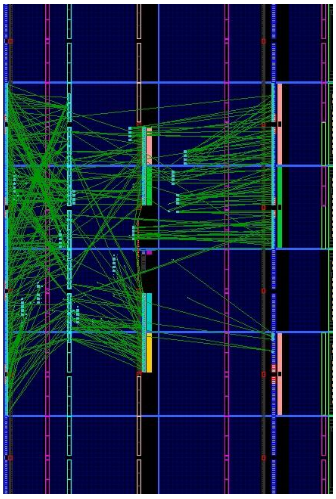


Figure 12. FPGA Editor of Channel

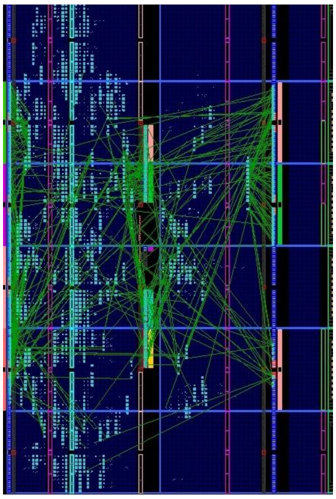


Figure 13. FPGA Editor of Receiver

From the Figure 11, 12 and 13, it can be observed that there are various connecting wires between different LUTs and FFs, which are in green colour. These are the input and output connecting wires.

5.2.2. SIMO

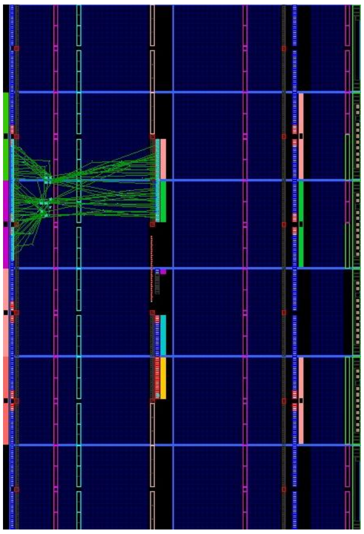


Figure 14. FPGA Editor of Transmitter

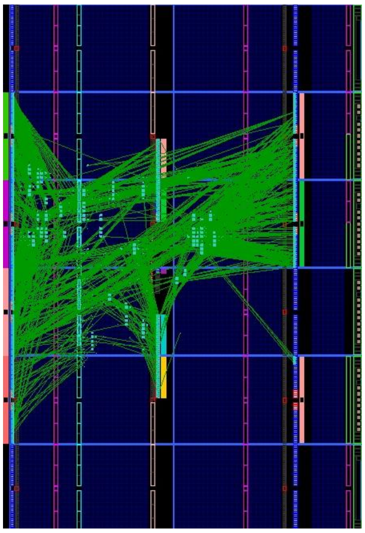


Figure 15. FPGA Editor of Channel

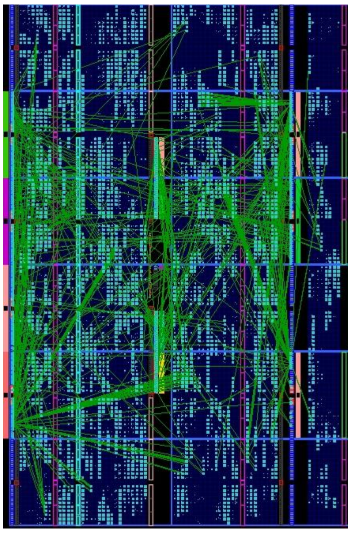


Figure 16. FPGA Editor of Receiver

From the Figure 14, 15 and 16, it can be observed that there are various connecting wires between different LUTs and FFs, which are in green colour. These are the input and output connecting wires.

5.3. RTL Schematic

RTL schematic is a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers , counters, AND gates, and OR gates.

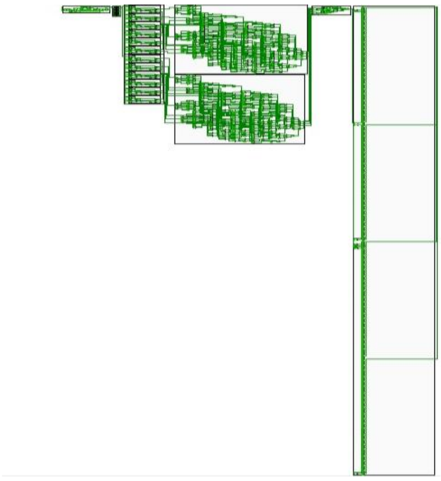


Figure 17. RTL Schematic of SISO

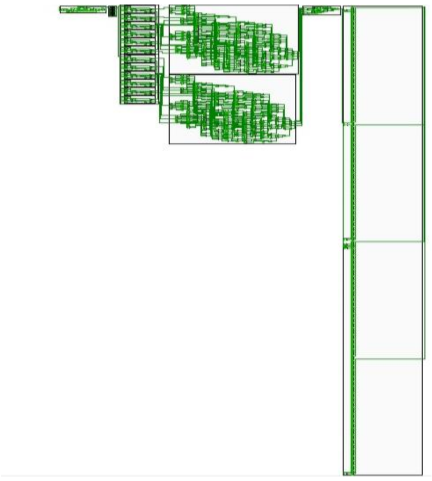


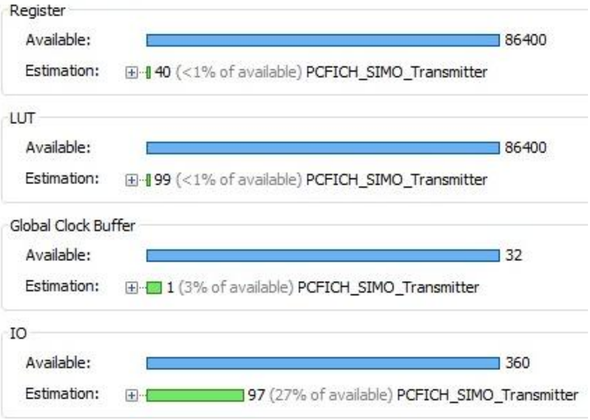
Figure 18. RTL Schematic of SIMO

Figure 17 and 18 shows the RTL Schematic of SISO and SIMO respectively.

5.4. Resource Estimation

Resource estimation indicates the amount of resources that got utilized by the device. In general, it indicates the number of Registers, LUT, Slice, I/O, Buffers utilized.

5.4.1. SISO



Register
Available: 86400
Estimation: 40 (<1% of available) PCFICH_SIMO_Transmitter

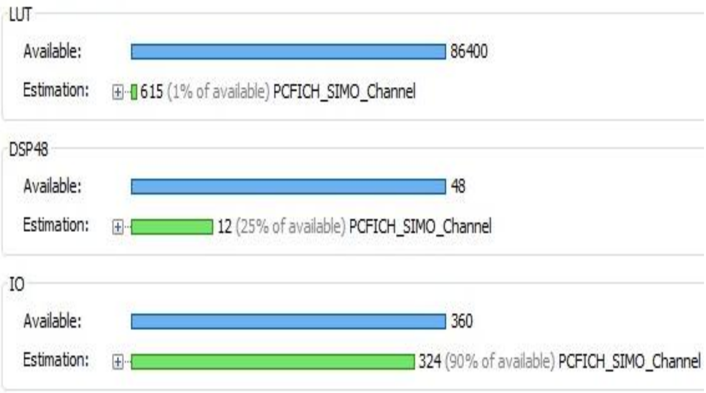
LUT
Available: 86400
Estimation: 99 (<1% of available) PCFICH_SIMO_Transmitter

Global Clock Buffer
Available: 32
Estimation: 1 (3% of available) PCFICH_SIMO_Transmitter

IO
Available: 360
Estimation: 97 (27% of available) PCFICH_SIMO_Transmitter

Figure 19. Resource Estimation of Transmitter

From the Figure 19, it can be seen that in the transmitter, the percentage of Registers consumed is 1%, LUT is 1% and IO is 27%.



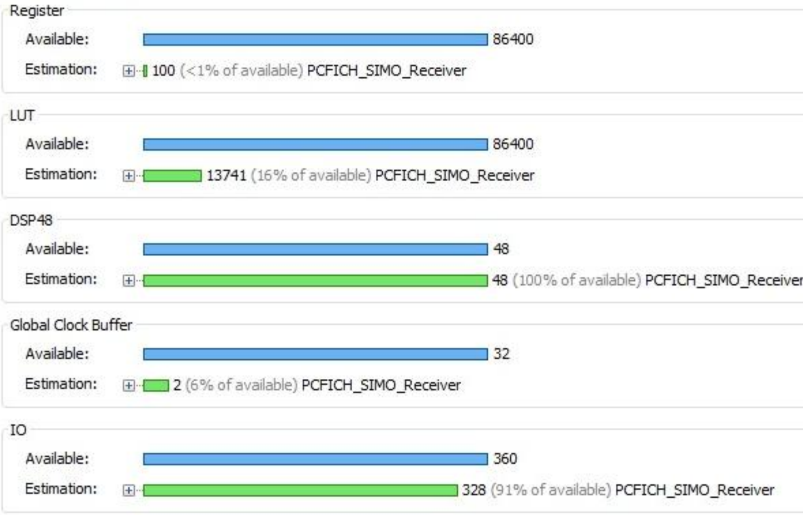
LUT
Available: 86400
Estimation: 615 (1% of available) PCFICH_SIMO_Channel

DSP48
Available: 48
Estimation: 12 (25% of available) PCFICH_SIMO_Channel

IO
Available: 360
Estimation: 324 (90% of available) PCFICH_SIMO_Channel

Figure 20. Resource Estimation of Channel

From the Figure 20, it is observed that in the channel, the percentage of LUT consumed is 1%, Slice is 25% and IO is 90%.



Register

Available: 86400

Estimation: 100 (<1% of available) PCFICH_SIMO_Receiver

LUT

Available: 86400

Estimation: 13741 (16% of available) PCFICH_SIMO_Receiver

DSP48

Available: 48

Estimation: 48 (100% of available) PCFICH_SIMO_Receiver

Global Clock Buffer

Available: 32

Estimation: 2 (6% of available) PCFICH_SIMO_Receiver

IO

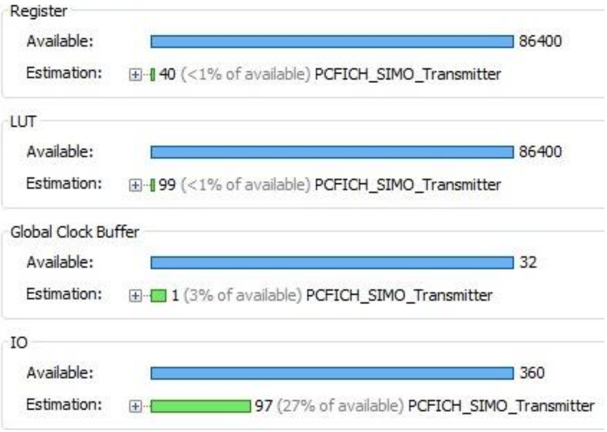
Available: 360

Estimation: 328 (91% of available) PCFICH_SIMO_Receiver

Figure 21. Resource Estimation of Receiver

From the Figure 21, it can be observed that in the receiver side, the percentage of Registers consumed is 1%, LUT is 16% and IO is 91%.

5.4.2. SIMO



Register

Available: 86400

Estimation: 40 (<1% of available) PCFICH_SIMO_Transmitter

LUT

Available: 86400

Estimation: 99 (<1% of available) PCFICH_SIMO_Transmitter

Global Clock Buffer

Available: 32

Estimation: 1 (3% of available) PCFICH_SIMO_Transmitter

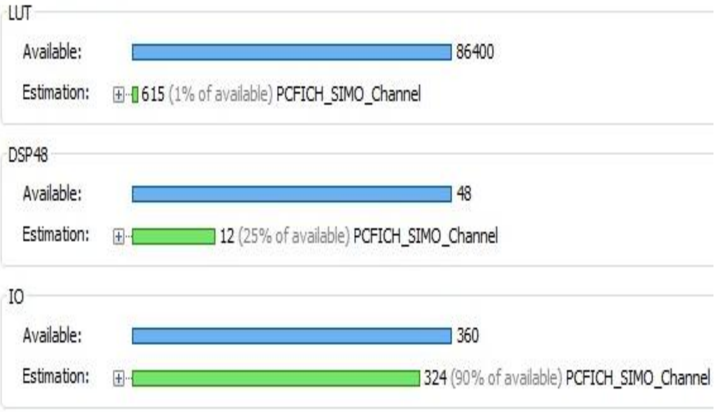
IO

Available: 360

Estimation: 97 (27% of available) PCFICH_SIMO_Transmitter

Figure 22. Resource Estimation of Transmitter

From the Figure 22, it can be observed that in the transmitter, the percentage of Registers consumed is 1%, LUT is 1%, Slice is 3% and IO is 27%.



LUT

Available: 86400

Estimation: ⊞ 615 (1% of available) PCFICH_SIMO_Channel

DSP48

Available: 48

Estimation: ⊞ 12 (25% of available) PCFICH_SIMO_Channel

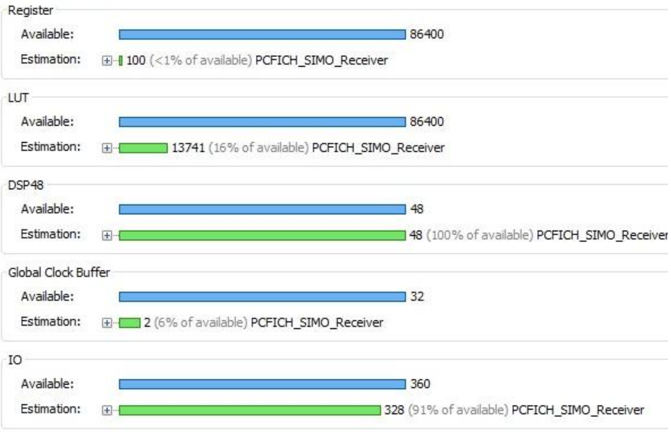
IO

Available: 360

Estimation: ⊞ 324 (90% of available) PCFICH_SIMO_Channel

Figure 23. Resource Estimation of Channel

From the Figure 23, it is seen that in the channel, the percentage of Registers consumed is 1%, LUT is 1%, Slice is 25% and IO is 90%.



Register

Available: 86400

Estimation: ⊞ 100 (<1% of available) PCFICH_SIMO_Receiver

LUT

Available: 86400

Estimation: ⊞ 13741 (16% of available) PCFICH_SIMO_Receiver

DSP48

Available: 48

Estimation: ⊞ 48 (100% of available) PCFICH_SIMO_Receiver

Global Clock Buffer

Available: 32

Estimation: ⊞ 2 (6% of available) PCFICH_SIMO_Receiver

IO

Available: 360

Estimation: ⊞ 328 (91% of available) PCFICH_SIMO_Receiver

Figure 24. Resource Estimation of Receiver

From the Figure 24, it can be observed that in the receiver side, the percentage of Registers consumed is 1%, LUT is 16% and IO is 91%.

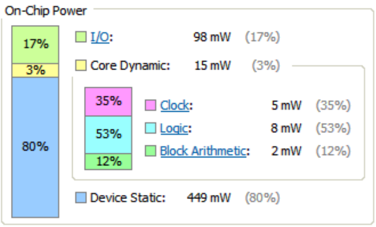
5.5. Power Estimation

Power estimation considers the design’s resource usage, toggle rates, I/O loading, and many other factors and it combines them with the device models to calculate the estimated power.

There are three types of power estimated in Xilinx:

- I/O Power - It is the power consumed due to external switching.
- Core Dynamic Power - It is the power consumed due to internal switching.
- Device Static Power - It is the power consumed when the device is powered up without programming the used logic. The main contributor of this is the junction temperature.

5.5.1. SISO



On-Chip Power

□ I/O: 98 mW (17%)

□ Core Dynamic: 15 mW (3%)

□ Clock: 5 mW (35%)

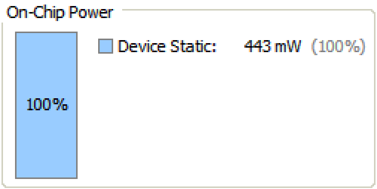
□ Logic: 8 mW (53%)

□ Block Arithmetic: 2 mW (12%)

□ Device Static: 449 mW (80%)

Figure 25. Power Estimation of Transmitter

From the Figure 25, it can be observed that the power consumed by I/O is 98mW, Core Dynamic is 15mW and Device Static is 449mW in the transmitter.

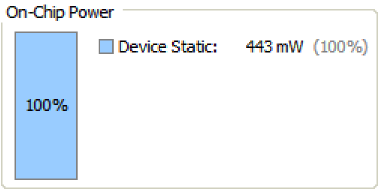


On-Chip Power

□ Device Static: 443 mW (100%)

Figure 26. Power Estimation of Channel

From the Figure 26, it is observed that the power consumed by Device Static is 443mW in the channel.



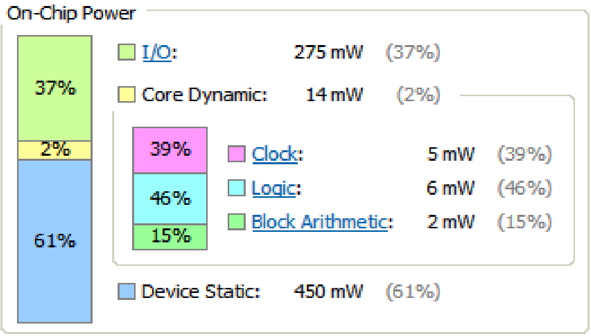
On-Chip Power

□ Device Static: 443 mW (100%)

Figure 27. Power Estimation of Receiver

Similarly, from the Figure 27, it can be observed that the power consumed by Device Static is 443mW in the receiver.

5.5.2. SIMO



On-Chip Power

□ I/O: 275 mW (37%)

□ Core Dynamic: 14 mW (2%)

□ Clock: 5 mW (39%)

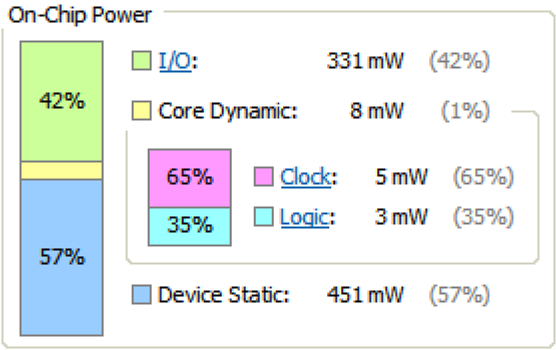
□ Logic: 6 mW (46%)

□ Block Arithmetic: 2 mW (15%)

□ Device Static: 450 mW (61%)

Figure 28. Power Estimation of Transmitter

From the Figure 28, it is observed that the power consumed by I/O is 275mW, Core Dynamic is 14mW and Device Static is 450mW in the transmitter.

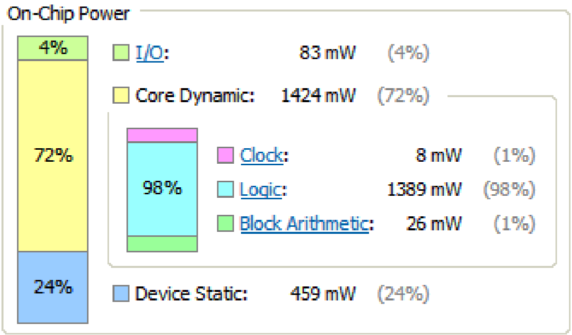


On-Chip Power

🟩 I/O:	331 mW	(42%)
🟨 Core Dynamic:	8 mW	(1%)
🟪 Clock:	5 mW	(65%)
🟦 Logic:	3 mW	(35%)
🟦 Device Static:	451 mW	(57%)

Figure 29. Power Estimation of Channel

From the Figure 29, it is seen that the power consumed by Device Static is 451mW in the channel.



On-Chip Power

🟩 I/O:	83 mW	(4%)
🟨 Core Dynamic:	1424 mW	(72%)
🟪 Clock:	8 mW	(1%)
🟦 Logic:	1389 mW	(98%)
🟩 Block Arithmetic:	26 mW	(1%)
🟦 Device Static:	459 mW	(24%)

Figure 30. Power Estimation of Receiver

Similarly, from the Figure 30, it is observed that the power consumed by Device Static is 459mW in the receiver.

5.6. Timing Summary

The timing summary indicates the overall period, input and output times. It is for all clocks and is limited by the slowest path. In Table 1, various timing parameters of SISO and SIMO are summarised.

Table 1. Timing Summary

Parameters	**SISO**	**SIMO**
Speed grade	-2	-2
Minimum period	1.430ns	2.527ns
Maximum frequency	699.301MHz	395.726MHz

5.7. Advanced HDL Synthesis Report

Advanced HDL synthesis report gives the correct technology map and interface to optimize the design. Table 2 and 3 shows the advanced HDL synthesis report of SISO and SIMO.

Table 2. Advanced HDL Synthesis Report of SISO

COMPONENTS	**TRANSMITTER**	**CHANNEL**	**RECEIVER**
ROMs	6	-	2
Multipliers	-	18	48
Adders/Subtractors	1	12	144
Counters	1	-	-
Registers	36	-	-
Latches	-	-	4
Comparators	-	-	6

Table 3. Advanced HDL Synthesis Report of SISO

COMPONENTS	**TRANSMITTER**	**CHANNEL**	**RECEIVER**
ROMs	6	-	2
Multipliers	-	24	96
Adders/Subtractors	1	60	288
Counters	1	-	-
Registers	36	-	-
Latches	-	-	4
Comparators	-	-	6

6. CONCLUSION

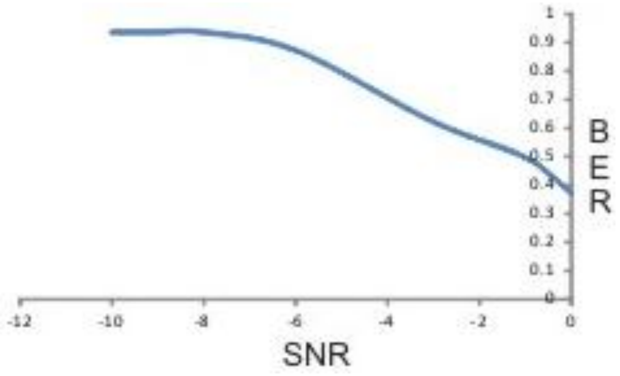


Figure 31. BER Vs. SNR

The output obtained for varying the variance is shown in the Figure 31. From the figure, it is observed that as the Signal-to-Noise Ratio increases, Bit Error Rate decreases. Similarly, channel emulators can be designed for MISO and MIMO environments under different channels like Rayleigh and Rician fading channels and their performance can be compared.

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I would like to thank God, my family and friends for being with me all the time.

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