

Revisiting the notion of Origin-Destination Traffic Matrix of the Hosts that are attached to a Switched Local Area Network

Monday Eyinagho¹, Samuel Falaki² and Anthony Atayero³

¹Department of Electrical and Information Engineering, Covenant University, Ota, Nigeria

eyimon@yahoo.com

²Department of Computer Science, Federal University of Technology, Akure, Nigeria

swolefalaki@yahoo.com

³Department of Electrical and Information Engineering, Covenant University, Ota, Nigeria

atayero@ieee.org

ABSTRACT

There is a widely held notion in the literature that there is an origin-destination traffic matrix for all the hosts (end nodes) that are attached to any switched local area network. This is usually in relation to the need to calculate the end-to-end (or maximum end-to-end) delays between all the end nodes that are attached to the network, for the sole purpose of using these delays values to design upper-bounded delay switched local area networks, in efforts at solving the delay problems of this class of networks. In this paper, we show that this notion of origin-destination traffic matrix for all the hosts that are attached to a switched local area network does not seem to be correct.

KEYWORDS

End-To-End Delay, Origin-Destination Pair, Switched Local Area Networks

1. INTRODUCTION

It is a widely held notion in the literature that to determine the average network delay of a switched Local Area Network (switched LAN), the traffic matrix of the hosts that are attached to the LAN has to be formulated. For example, in [1], it was stated that, let T_{ij} denote the information flow in packets per unit time between end nodes i and j of the network; we define the traffic matrix of the network to be the $n \times n$ matrix $T = (T_{ij})$ where n is the number of end nodes. Moreover, in [2], the average end-to-end delay time of a switched local area network was defined with respect to the average traffic between end node i and end node j for all end nodes that are attached to the LAN and the average delay between the end nodes was defined as the weighted combination of all end-to-end delay times. Elbaum and Sidi on the other hand in [3] defined minimum average network delay as the average delay between all pairs of users in the network. In this paper, we show that this notion of origin-destination traffic matrix for all hosts that are attached to a switched local area network with a view to using it to compute end-to-end delays (or average end-to-end delay) does not seem to be correct.

2. ANALYSIS OF SWITCHED LOCAL AREA NETWORKS' ORIGIN-DESTINATION TRAFFIC ENUMERATION METHOD USING THE HOSTS THAT ARE ATTACHED TO THE NETWORK

For packet switched [4 p.366], random access [5], lossless [4, p.366], [5] networks, offered load = throughput, but,

$$\text{throughput} = \frac{\text{amount of data transferrd}}{\text{time taken to effect the transfer}} \text{ therefore,}$$

$$\text{offered load} = \frac{\text{amount of data transferrd}}{\text{time taken to effect the transfer}}$$

For any origin-destination pair of nodes (hosts),
time taken to effect the transfer = delay from origin node (host) to destination node (host)

maximum time to effect the transfer = maximum delay from origin host to destination host

maximum time to effect the transfer from origin host to destination host = maximum time (delay) through the 1st switch + maximum time (delay) through the 2nd switch + ...+ maximum time (delay) through the nth switch on the origin-destination path

If an external site presents to the origin-destination path (route) Z packets every second (loading or offered load), then it presents 1 packet every $\frac{1}{Z}$ seconds.

Since for a lossless system, offered load = throughput,
maximum time to effect the transfer of 1 packet = maximum delay from origin host to destination host of 1 packet

$$= \text{maximum time (delay) through 1}^{\text{st}} \text{ switch} + \text{maximum time (delay) through 2}^{\text{nd}} \text{ switch} + \dots + \text{maximum time (delay) through n}^{\text{th}} \text{ switch} \leq \frac{1}{Z} \quad (1)$$

where n = the number of switches in the origin-destination path (route).

The \leq inequality symbol in (1) implies that $\frac{1}{Z}$ seconds is an upper bound on end-to-end delay

for the origin-destination pair of hosts. Above $\frac{1}{Z}$ seconds, we will have a loss system. Therefore,

since we are interested in the maximum (upper bounded) delay, the \leq symbol in (1) can be replaced by an = symbol and hence, (1) becomes an equation.

We can also rationalize the preceding idea in this way. Consider an origin-destination pair of hosts that are involved in a communication session. Let us assume that the local area network (LAN) is a switched Ethernet LAN.

Assume that X Megabits/sec (Mbps) = maximum Ethernet port transfer rate of a host,

$$= \frac{X}{(\text{minimum Ethernet packet length})} \text{ packets/sec.} \quad (2)$$

= Z packets/sec, say.

Or, it transfers 1 packet every $\frac{1}{Z}$ seconds.

The minimum Ethernet packet length should be used in (2) because, this will give us the maximum packets/sec. (maximum loading) and hence, it will give us an upper bounded delay situation. Therefore, for a lossless system, each packet should cross all the switches in its path from origin-to-destination in $\frac{1}{Z}$ seconds. This idea was succinctly expressed by Bersekas and Gallagar in [4, p.511]; where it was stated that, a strict implementation of a communication session's rate of r packets/sec. would be to admit 1 packet every $\frac{1}{r}$ seconds. As an example, for hosts (workstations), X could be 10Mbps (mega bits per second) or the basic Ethernet rate, 100Mbps (Fast Ethernet rate). For Servers, X could be 1,000Mbps (Gigabit Ethernet rate).

Consider a network that has two (2) hosts connected by a switch as shown in Figure 1.

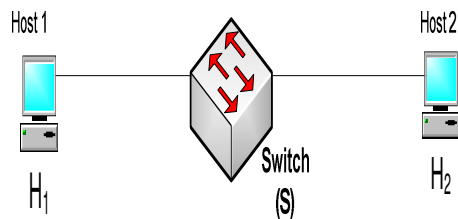


Fig. 1 Two hosts connected through one switch

We can see that either of the hosts will be sending data traffic to the other host or receiving data traffic from it; therefore, we will have the traffic matrix shown in (3).

$$\begin{bmatrix} \cancel{11} & 21 \\ 12 & \cancel{22} \end{bmatrix} \tag{3}$$

12 is Host1 sending data traffic to Host2 and Host2 receiving data traffic from Host1; similarly, 21 is Host2 sending data traffic to Host1, and Host1 receiving the traffic. 11 is Host1 sending data traffic to itself (which is not possible); and 22 is Host2 sending data traffic to itself (which is also not possible). Therefore, the diagonal entries are not necessary, but we retain them so that we can get a correct picture of the network traffic matrix; the diagonal entries are hence, crossed out. But we can see from Figure 1 and from (3) that end-to-end delay in the direction from Host1 to Host2 is the same as the end-to-end delay from Host2 to Host1; so for a two (2) hosts network, we need 1 end-to-end delay, since: end-to-end delay 12 = end-to-end delay 21.

Consider also, a network that has three (3) hosts. There are more than one ways of connecting the hosts. It may be through a switch or through multiple switches (this again can have multiple configurations). We illustrate just two of the configurations in Figures 2 and 3. We should emphasize at this point that, in our illustrations (Figures.1, 2, and 3) and indeed in any LAN installation, one or more of the hosts may be a server or servers (for example, file server, web server); but for the purpose of our analysis, we regard all connected end devices (computing devices, printing devices and others) as hosts.

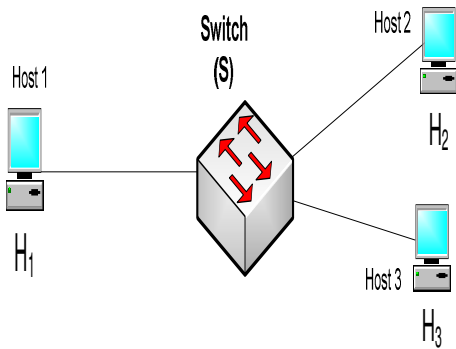


Fig. 2 Three hosts connected through one switch

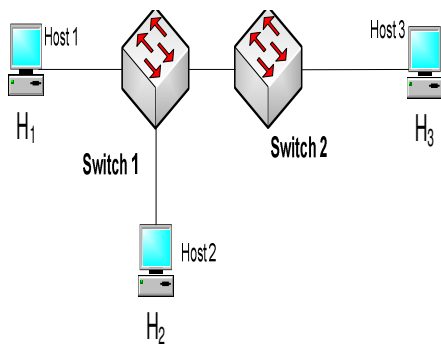


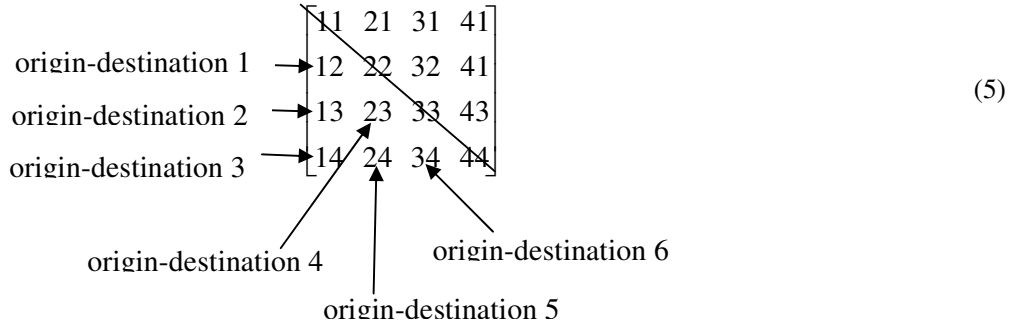
Fig. 3 Three hosts connected through two switch

What ever be the configuration (connection) of the three hosts network does not matter; what is important in the context of our analysis is that, Host1 can either be sending traffic to Host2 or receiving traffic from Host2, it can either be sending traffic to Host3 or receiving traffic from Host3. The same scenario holds for Host2 and Host3. We therefore, have the traffic matrix for a three (3) hosts connected through two (2) switches network as shown in (3).

$$\begin{bmatrix} 11 & 21 & 31 \\ 12 & 22 & 32 \\ 13 & 23 & 33 \end{bmatrix} \tag{4}$$

Following our previous explanations, we cross out the diagonal entries. Also, since the traffic from Host1 to Host2 will cross the same number of switches from origin to destination, as the traffic from Host2 to Host1, it follows that, end-to-end delay 12 = end-to-end delay 21. Similarly, end-to-end delay 13 = end-to-end delay 31, end-to-end delay 23 = end-to-end delay 32. Therefore, for a three (3) hosts network, we need 3 end-to-end delays. By following the preceding explanations, we can proceed to write out the traffic matrix for a four (4) hosts' network as shown in (5).

By similar reasoning, we can see that for a four (4) hosts' network, we need 6 end-to-end delays. Following the same logic, we can show that for a five (5) hosts network, we need 10 end-to-end delays, for a six (6) hosts network, we need 15 end-to-end delays.



We have been able to come-up with a closed-form relation for finding the number of end-to-end delays (number of origin-destination pairs) to be used with inequality (1) (in inequality (1), we have considered only one (1) origin-destination pair of two (2) hosts involved in a communication session) for any switched LAN. For a switched LAN, if,

p = the LAN's number of end-to-end delays (with respect to attached hosts or end nodes),
 k = number of end nodes (hosts) in the LAN, then,

$$p = \sum_{x=1}^{k-1} (k-x) \tag{6}$$

For example, if k = 3, $p = \sum_{x=1}^{3-1} (3-x) = \sum_{x=1}^2 (3-x) = (3-1) + (3-2) = 2+1 = 3$

No matter the number of hosts that are attached to the LAN, we can calculate the number of end-to-end delays (number of origin host to destination host delays) with respect to (1) by using (6).

Consider the three (3) hosts, two (2) switches LAN shown in Figure 3. Since the application of (6) gives us three origin-destination pairs, and from (1) the 3 origin-destination pairs of hosts are 1-2, 1-3, and 2-3. For this network therefore, the three origin-destination equations (using (1) which has an upper bound of $\frac{1}{Z}$) are:

For the 1-2 origin-destination pair of hosts,
 maximum time to transfer 1 packet from H₁ to H₂ (maximum end-to-end delay) =
 max. time (delay) through switch 1 = $\frac{1}{Z_1}$ (7)

For the 1-3 origin-destination pair of hosts,
 maximum time to transfer 1 packet from H₁ to H₃ (maximum end-to-end delay) =
 max. time (delay) through switch 1 + max. time (delay) through switch 2 = $\frac{1}{Z_2}$ (8)

For the 2-3 origin-destination pair of hosts,
 maximum time to transfer 1 packet from H₂ to H₃ (maximum end-to-end delay) = max. time (delay) through switch 1 + max. time (delay) through switch 2 = $\frac{1}{Z_3}$ (9)

where Z₁, Z₂, and Z₃ are the Ethernet port transfer rates in packets per second of any of the two hosts that are involved in a communication session in (7), (8), and (9) respectively. We can write out (7), (8), and (9) together in matrix form as:

$$\begin{bmatrix} \text{origin/destination12 maximum end-to} \\ \text{-end delay} \\ \text{origin/destination13 maximum end-to} \\ \text{-end delay} \\ \text{origin/destination23 maximum end-to} \\ \text{-end delay} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \\ 1 & 1 \end{bmatrix} \times \begin{bmatrix} \text{max imum delay of} \\ \text{any data packet} \\ \text{through switch1} \\ \text{max imum delay of} \\ \text{any data packet} \\ \text{through switch 2} \end{bmatrix} \quad (10)$$

Where an entry in the bit matrix is 1 if a packet from or to any of the hosts at either ends in the origin-destination path (the maximum end-to-end delay entry of the maximum end-to-end delay column vector) crosses the corresponding switch in transiting from origin host to destination host; the entry is 0, if the packet does not cross the switch. We can re-write (10) as in (11); where $a_{11} = a_{21} = a_{22} = a_{31} = a_{32} = 1$ and $a_{12} = 0$. Matrix Eq. (11) can be written for any switched local area network, with any arbitrary number of m switches and k hosts.

Let $y_1, y_2, y_3, \dots, y_{p-1}, y_p$ represent origin-destination pair1 maximum end-to-end delay, origin-destination pair2 maximum end-to-end delay, origin-destination pair3 maximum end-to-end delay, ..., origin destination pair p-1 maximum end-to-end delay and origin-destination pair p maximum end-to-end delay respectively.

$$\begin{bmatrix} \text{origin/destination12 maximum end-to} \\ \text{-end delay} \\ \text{origin/destination13 maximum end-to} \\ \text{-end delay} \\ \text{origin/destination23 maximum end-to} \\ \text{-end delay} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \\ a_{31} & a_{32} \end{bmatrix} \times \begin{bmatrix} \text{max imum delay of} \\ \text{any data packet} \\ \text{through switch 1} \\ \text{max imum delay of} \\ \text{any data packet} \\ \text{through switch 2} \end{bmatrix} \quad (11)$$

Also, let $x_1, x_2, x_3, \dots, x_{m-1}, x_m$ represent the maximum delay of any data packet through switch 1, the maximum delay of any data packet through switch 2, the maximum delay of any data packet through switch 3, ..., the maximum delay of any data packet through switch m-1, the maximum delay of any data packet through switch m respectively, then (11) can be written for any switched local area network as in (12).

$$\begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ \dots \\ \dots \\ \dots \\ y_{p-1} \\ y_p \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \dots & a_{1m-1} & a_{1m} \\ a_{21} & a_{22} & \dots & a_{2m-1} & a_{2m} \\ a_{31} & a_{32} & \dots & a_{3m-1} & a_{3m} \\ \dots & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & \dots \\ a_{p-11} & a_{p-12} & \dots & a_{p-1m-1} & a_{p-1m} \\ a_{p1} & a_{p2} & \dots & a_{pm-1} & a_{pm} \end{bmatrix} \times \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ \dots \\ \dots \\ \dots \\ x_{m-1} \\ x_m \end{bmatrix} \quad (12)$$

where $y_1 = \frac{1}{Z_1}, y_2 = \frac{1}{Z_2}, \dots, y_p = \frac{1}{Z_p}$ and $x_1, x_2, x_3, \dots, x_{m-1}, x_m$ are the unknown.

m = number of switches in the local area network;

$a_{ij} = 1/0, i = 1,2,3,\dots,p; j = 1,2,3,\dots,m$ are elements of the path bit matrix for the whole network.;

$a_{ij} = 1$, if a data packet that transverses origin-destination i passes through switch j ;

$a_{ij} = 0$, if a data packet that transverses origin-destination i does not pass through switch j ;

p = the LAN's number of origin-destination pairs of hosts, which is given by (6).

Put in compact form, (12) can be written as:

$$\underline{y} = A\underline{X} \tag{13}$$

Where A is the $p \times m$ matrix, $X = (x_1, x_2, x_3, \dots, x_{m-1}, x_m)$ is a $1 \times m$ column vector, and $\underline{y} = (y_1, y_2, y_3, \dots, y_{p-1}, y_p)$ is a $1 \times p$ column vector in (12) respectively.

On the surface, (12) seems to support the notion that there is an origin-destination pairs traffic matrix with respect to end-to-end delay computation for all the hosts that are attached to a switched LAN as enunciated (we think, not correctly) in [1], [2], [6]. We now explain why this notion does not seem to be correct when applied to switched LANs.

If we look at (10), we see that rows 2 and 3 of the bit matrix have the same type of entries, indeed $a_{21} = a_{31}$ and $a_{22} = a_{32}$ in relation to (11). This will make the set of vectors resulting from (11) to be linearly dependent. If (12) is written out for (11), we will have (14). Carrying out matrix multiplication on (14) will result in the system of equations as shown in (15).

$$\begin{bmatrix} y_1 \\ y_2 \\ y_3 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \\ a_{31} & a_{32} \end{bmatrix} \times \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{14}$$

$$y_1 = a_{11}x_1 + a_{12}x_2 \tag{15a}$$

$$y_2 = a_{21}x_1 + a_{22}x_2 \tag{15b}$$

$$y_3 = a_{31}x_1 + a_{32}x_2 \tag{15c}$$

The reason for the linear dependence of the system of equations in (15) is that, if we look at the network of Figure 3, for host H_1 to communicate with host H_3 , and vice versa, data packets will transit through switch 1 and switch 2; the same thing as when host H_2 is to communicate with host H_3 or H_3 with H_2 . Therefore, the maximum delays of a data packet in switch 1 and switch 2 for the two communication sessions are the same; hence, the similarity of the entries in rows 2 and 3 of the end-to-end paths bit matrix in (10).

In the words of Kreyzig in [7, p.332], ‘what is the point of linear independence and dependence?’ And he provided the following answer: ‘well, from a linearly dependent set of vectors, we may often omit vectors that are linear combination of others until we are finally left with a linearly independent subset of the ‘really essential’ vectors, which can no longer be expressed linearly in terms of each other’ [7, p.332]. Therefore, if we eliminate the linearly dependent set of vectors from (14), some of the y_i 's will vanish; meaning that the communication paths of some of the hosts (origin-destination pairs of hosts) will vanish. This is because packets travelling between two end hosts will suffer maximum delays in the same set of switches along their end-to-end paths. This proves the fact (and we are proposing a new theory) that there is no origin-destination pairs traffic matrix with respect to end-to-end delay computation for all the hosts that are attached to a switched local area network.

3. CONCLUSIONS

We have shown in the context of computing the end-to-end (or maximum end-to-end) delays of switched local area networks that there is no origin-destination pair traffic matrix for all the hosts that are attached to any of such networks. We have therefore, proposed the theory that, there is no origin-destination pairs traffic matrix with respect to end-to-end delay computation for all the hosts that are attached to a switched local area network. How then do we enumerate all the end-to-end delays of any switched local area network, in order to be able to calculate, for example, the network average of maximum end-to-end delays? This can be used to design an upper bounded delay switched local area network. A methodology for enumerating all the end-to-end delays of any switched local area network will be reported in another paper.

REFERENCES

- [1] P. Torab & E. Kamen (1999) "Load Analysis of Packet Switched Networks in Control Systems", Proceedings 25th Annual Conference of the IEEE Industrial Electronics Society, San Jose, CA, vol. 3, pp.1222 – 1227.
- [2] E., Kanem, P. Torab, K. Cooper & G. Custodi (1999) "Design and Analysis of Packet Switched Networks for Control Systems", Proceedings IEEE Conference on Decision and Control, Phoenix, AZ, pp. 4460-4465.
- [3] R. Elbaum & M. Sidi (1996) "Topological Design of Local Area Networks using Genetic Algorithms", IEEE Transactions on Networking, vol.4, no.5, pp.766-778.
- [4] D. Bertsekas & R. Gallager (1992) Data Networks, Prentice-Hall, Englewood Cliffs, USA.
- [5] M. Reiser (1982) "Performance Evaluation of Data Communications Systems", Proceedings of the 1982 IEEE Conference, vol. 70, no. 2, pp.171-194.
- [6] N. Krommenacker, E. Rondeau, & T. Divoux (2001) "Study of Algorithms to Define the Cabling Plan of Switched Ethernet for Real-Time Applications", Proceedings of the 8th IEEE International Conference on Emerging Technologies and Factory Communications, Antibes, pp.223-230
- [7] E. Kreyzig (2003) Advanced Engineering Mathematics, 8th Edition, John Wiley and Sons, New York, USA.



Monday Ofori Eyinagho obtained a B. Sc. Degree in Electronic and Electrical Engineering from the Obafemi Awolowo University, Ile-Ife, Nigeria in 1988. He also holds a Post-Graduate Diploma in Computer Science from the University of Lagos, Lagos, Nigeria (1991), an MBA (General Management) Degree from the River State University of Science and Technology, Port-Harcourt, Nigeria (2003), an M.Sc Degree in Computer Engineering, from the Federal University of Technology, Owerri, Nigeria (2004), and a Ph. D in Computer Engineering from Covenant University, Ota, Nigeria (2011). Dr. Eyinagho has had extensive industrial work experience in a number of corporate organizations. He is currently a Lecturer in the Department of Electrical and Information Engineering, Covenant University, Ota, Nigeria. Dr. Eyinagho has published scholarly papers in international journals. He is a member of The Nigerian Society of Engineers, a COREN Registered Electronics Engineer, and member Nigeria Computer Society. His principal researches are in the areas of developing and implementing microprocessor-based systems and performance optimization of local area networks.



Oluwole Samuel Falaki is a Professor of Computer Engineering at the Federal University of Technology, Akure, Nigeria. He holds an M. Eng Degree in Electrical Engineering from Leningrad University, an M. Sc Degree in Computer Science from UCLA and a Ph.D in Electrical Engineering from the University of Lagos, Lagos, Nigeria. His research interests are in the areas of Computer Architecture, Computer Communications and Networking, Network Security and Digital Signal Processing. He is a Fellow of the Nigeria Computer Society, Member of the Nigerian Society of Engineers, Member of IEEE and Member of ACM.



Aderemi A. Atayero is a Senior Lecturer in the Department of Electrical and Information Engineering, Covenant University, Ota, Nigeria. He graduated from the Moscow Institute of Technology (MIT) with a Bachelor of Science Degree in Radio Engineering and a Master of Science Degree in Satellite Communication Systems in 1992 and 1994 respectively. He received a Ph.D from the Moscow State Technical University of Civil Aviation (MSTUCA) in 2000. Dr. Atayero is a member of the Institute of Electrical and Electronic Engineers. He has published a number of scientific papers in International peer-reviewed journals and proceedings. He has served as the Head of Department of Electrical and Information Engineering at Covenant University. He is on the editorial board of the Covenant Journal of Science and Technology. He is a recipient of the '2009 Ford Foundation Teaching Innovation Award'. His current research interests are in Information Theory and Stochastic Self-Similar Processes and their applications in telecommunications.