DESIGN OF LOW POWER AND HIGH SPEED INVERTER

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ABSTRACT

The extensive growth of battery operated devices has made low-power design important in recent years. As electronics are being integrated into portable devices, the demand grows for increased functionality, with reduced size and long battery life. This implies a need to balance ultra-low power with area-efficient design. An obvious way to minimize energy per operation is to decrease VDD. This decreases active power, as well as leakage power, which is affected by DIBL. If VDD is decreased too sharply, however, increased delay time causes the power-delay product (PDP) to rise, can be kept minimum if operated in Subthreshold region. In this paper the advantages of the subthreshold inverter compared to the conventional strong inversion inverter with 90 nm technology in Cadence is presented.

KEYWORDS

Subthreshold region, Power-Delay Product, DIBL, Temperature.

1. INTRODUCTION

As growth in technology and use of mobile applications, power consumption has become one of the major attractions in circuit design. As technology scales deeper into the sub-micron designs, traditional CMOS gates present more and more substantial leakage currents [1]. While this is acceptable when trying to achieve the highest possible performance in presence of an unlimited power supply, but same can't be with battery operated mobile devices that need to operate for extended periods without recharging.

While dealing with low frequency applications, circuits operating in the subthreshold region have been shown to be the ideal choice [2]. Recently, with growing needs for low-power consumption, minimal energy circuits have become more attractive. Operation in the Subthreshold or weak-inversion region exploits the parasitic subthreshold leakage current, and uses it as primary operating current. These currents are much weaker than standard strong-inversion currents, and so the time needed for charging or discharging capacitive nodes is longer, limiting the operation frequency of the circuit. Subthreshold operation can substantially reduce both static and dynamic power consumption [3]. Dynamic power is greatly reduced, primarily due to the quadratic dependency on supply voltage, while static subthreshold leakage is also much lower, mainly because of the Drain-Induced Barrier Lowering (DIBL) effect. Accordingly, it could be concluded that a simple reduction of supply voltage of traditional circuits would achieve subthreshold operation. The characteristics of semiconductor behaviour in weak inversion are different than those in strong inversion, resulting in different sizing and ratio optimizations. This short paper briefly presents the concept of subthreshold operation and comparisons of PDP at different voltages and Delay at different temperatures is shown through simulations in advanced CMOS processes, such as 90nm.

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2. CHARACTERISTICS OF nMOS AND pMOS

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. For an n-channel MOSFET, the three operational modes are:

1. Cut-off, subthreshold, or weak-inversion mode, When $V_{GS} < V_{th}$
2. Triode mode or linear region, When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$
3. Saturation or active mode, When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$

In this paper, the simulations are performed in CADENCE Design tool. And the schematic diagrams are drawn in virtuoso schematic editor using 90nm technology file.

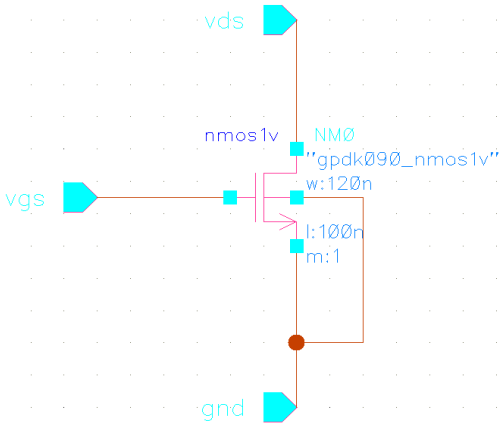

Figure 1. NMOS Transistor

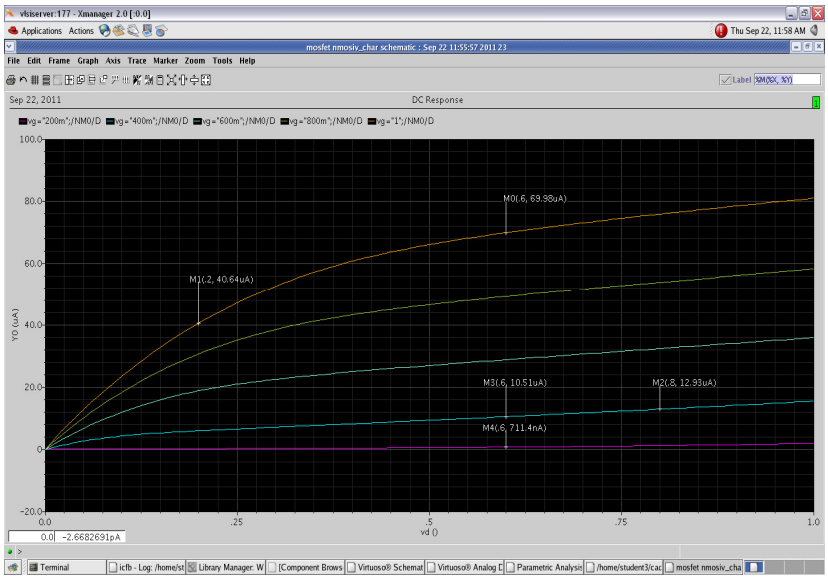

Figure 2. I-V Characteristics of NMOS

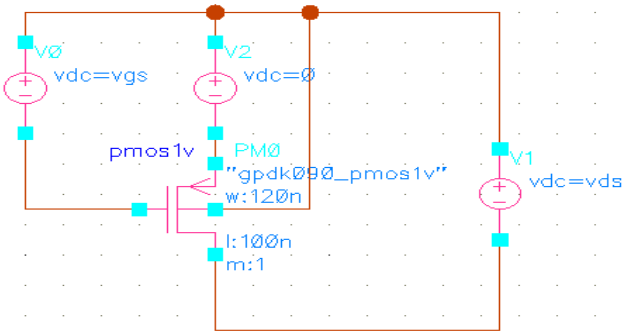

Figure 3. PMOS Transistor

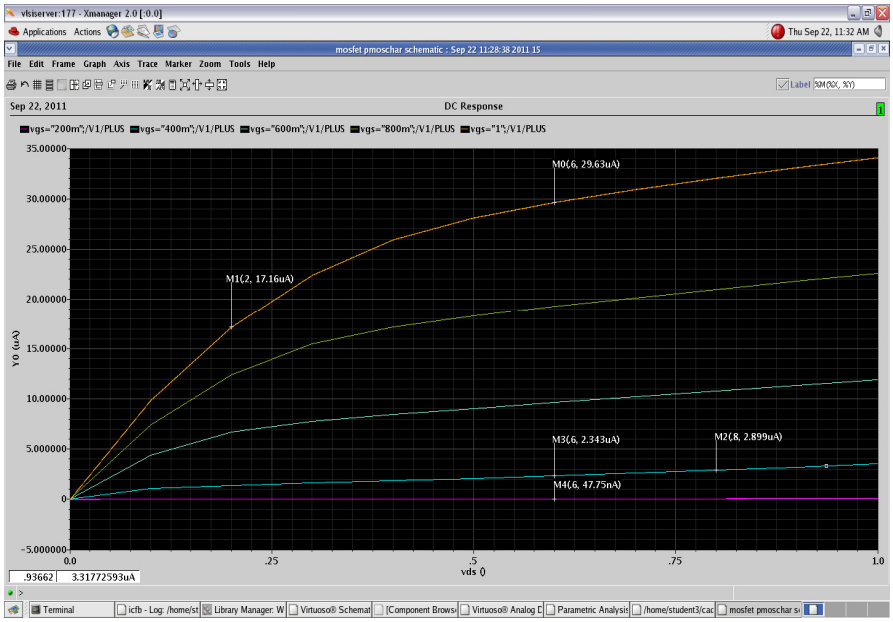

Figure 4. I-V Characteristics of PMOS

Figure 2 and Figure 4 are the characteristics drawn between I_{DS} and V_{DS} by sweeping the value of V_{GS} with a step size of 0.2V from 0.2V to 1V.The values taken are based on the operating regions of MOSFET at different applied voltages and corresponding Drain Currents are observed in Table 1 and Table 2 respectively.

3. CMOS INVERTER

3.1. CONVENTIONAL CMOS INVERTER

The inverter is truly the nucleus of all digital designs. The electrical behaviour of complex circuits can be almost completely derived by extrapolating the results obtained for inverters. Figure 5 shows the circuit diagram of a static CMOS inverter. When Vin is high and equal to VDD, the NMOS transistor is on, while the PMOS is off. A direct path exists between Vout and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), NMOS and PMOS transistors are off and on, respectively. A path exists between VDD and Vout, yielding a high output voltage. The gate clearly functions as an inverter. [5]

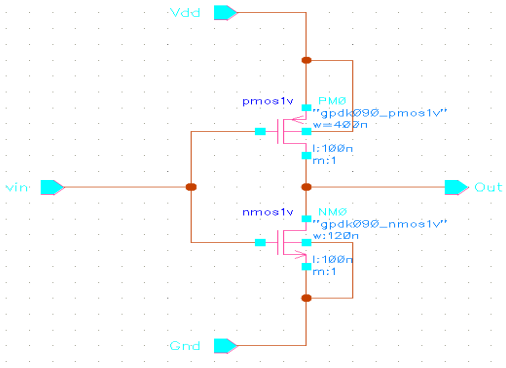

Figure 5. Conventional CMOS Inverter

3.2. SUBTHREHOLD CMOS INVERTER

The Subthreshold region of operation for an MOS transistor occurs when the gate-to-source voltage (V_{GS}) of the transistor is biased under the threshold voltage (V_{TH}). Showing the drain current (I_D) vs. V_{GS} curve (see Figure 6.) on a logarithmic scale shows that the current decays exponentially when V_{GS} is below V_{TH}. In a long channel device, V_{TH} neither depends on the channel length nor drain bias. However, in sub-micron technologies source and drain depletion regions penetrate significantly into the channel and control the potential and the field inside the channel. The Subthreshold current of an MOS device, taking into account is given by equation 1 [4]:

$$I_{DS} = 2n\mu_0 C_{ox} \frac{W}{L}\left[\frac{kT}{q}\right]^2 e^{\frac{V_{gs}-V_T}{nkT/q}}\left[1-e^{\frac{-V_{DS}}{kT/q}}\right] \qquad (1)$$

$$= I_s e^{\frac{V_{gs}-V_T}{nkT/q}}\left[1-e^{\frac{-V_{DS}}{kT/q}}\right]$$

$$S = n\left[\frac{kT}{q}\right]\ln(10) \qquad (2)$$

where V_{GS} is transistor gate to source voltage, V_{DS} is transistor drain to source voltage, V_{TH} is threshold voltage, n is the slope factor of the MOSFET, μ_0 is zero bias mobility, C_{ox} is gate oxide capacitance, W and L are the width and length of the MOSFET, S is the subthreshold swing.

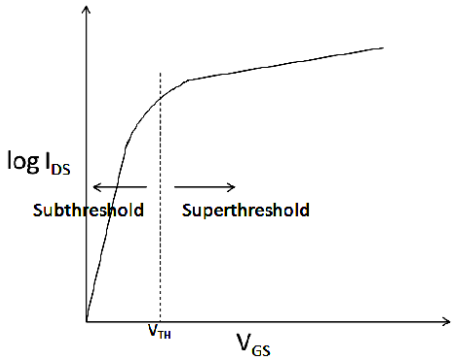

Figure 6. log IDSVs VGS Curve

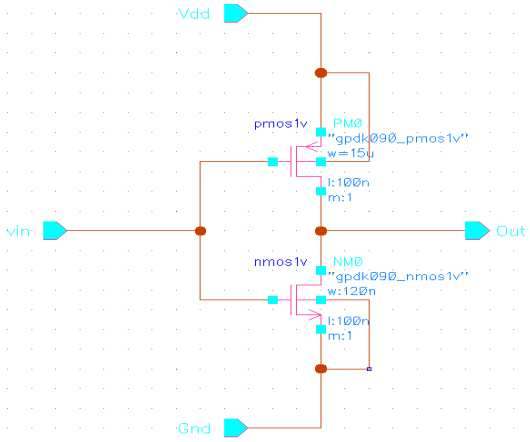

Figure 7. Subthreshold CMOS Inverter

4. PRACTICAL OBSERVATIONS

4.1. CALCULATION OF V_T FOR NMOS AND PMOS

The output characteristics of both nMOS and pMOS are shown in the figures 2 and 4.From the observation of both the characteristics, and using the values, the process parameters can be calculated as shown.

Table 1. Current at different operating regions in NMOS

EXP.No	V_{GS}(V)	V_{DS}(V)	I_D(µA)	Region of operation
1	1	0.6	69.98	Velocity saturation
2	1	0.2	40.64	Linear
3	0.4	0.8	12.93	Saturation
4	0.4	0.6	10.51	Saturation
5	0.2	0.6	0.7114	Saturation

Table 2. Current at different operating regions in PMOS

EXP.No	V_{GS}(V)	V_{DS}(V)	I_D(µA)	Region of operation
1	1	0.6	29.63	Velocity saturation
2	1	0.2	17.16	Linear
3	0.4	0.8	2.899	Saturation
4	0.4	0.6	2.343	Saturation
5	0.2	0.6	0.0477	Saturation

By using [5],

$$I_D = k' \frac{W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad \textbf{(3)}$$

We have calculated the following parameters of both NMOS and PMOS using Cadence in 90nm technology.

Table 3. Parameters in 90 nm Technology

	V_{TH}(V)	$\lambda(V^{-1})$	$k'(\mu A/V^2)$	V_{sat}(V)	S (Subthreshold Swing)
nMOS	0.13	3.71	74.5	0.35	101mv/dec
pMOS	-0.16	-3.9	-21.4	-0.77	70mv/dec

Table 4. Comparison of Delay, Avg. Power and PDP at different voltages at 27^0C

V_{DD} (V)	Dealy $(t_p)(10^{-9})$	Average power$(P_a)(10^{-9})$	PDP $(t_p * P_a)$ (10^{-18})
0.1	71.5792	0.402038	28.7775
0.12	44.7912	0.582717	26.1005
0.13	35.6793	0.684406	24.4191
0.14	28.1422	0.795830	22.3964
0.15	22.4041	0.914164	20.4809
0.16	17.8550	1.03961	18.5622
1	0.0768545	39.5849	3.04227

Table 5. Delays at different temperatures

V_{DD}(V)	27^0C	40^0C	60^0C
0.1	7.15792E-08	5.77475E-08	4.31790E-08
0.12	4.47912E-08	3.77300E-08	2.93800E-08
0.20	1.90740E-09	1.62700E-09	1.27820E-09
0.40	4.15200E-11	4.16000E-11	4.15820E-11
0.60	1.37225E-11	1.40950E-11	1.47460E-11
0.80	8.25200E-12	9.18780E-12	9.64620E-12
1.00	7.68545E-11	9.37320E-12	7.59980E-12

4. RESULTS

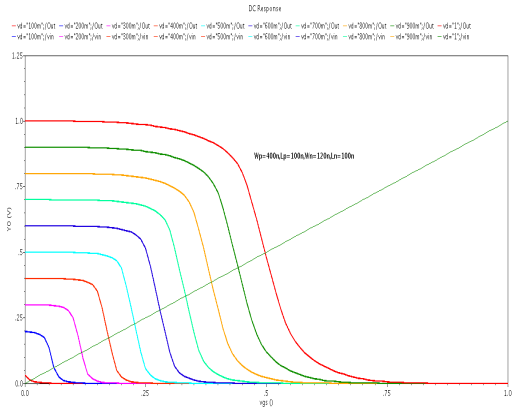

Figure 8. VTC as function of supply voltage (Wp =400n)

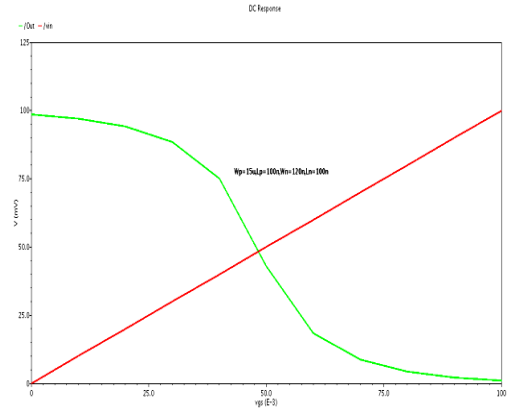

Figure 9. VTC in subthreshold region (Wp=15u)

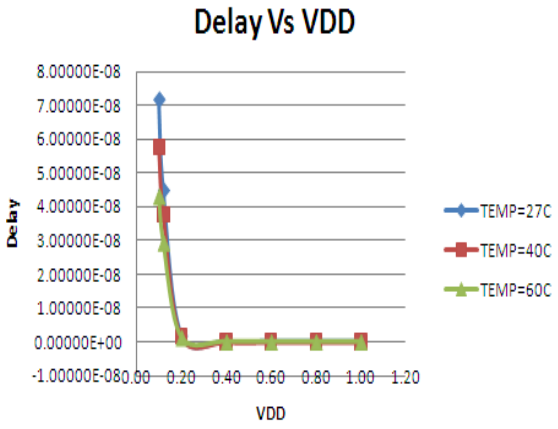

Figure 10. Delay Vs VDD at different Temperatures

Observing the Figure 8, the logic'1'degradation occurs for Wp = 400nm in the subthreshold region. This can be avoided by selecting Wp is 15um and the VTC curve is obtained as shown in the Figure 9 for subthreshold region.The Figure 10 shows the

relation between Delay Vs VDD for temperatures 27^0C, 40^0C and 60^0C. It is observed, as the temperature increases the Delay decreases which results in the increased speed of operation.

5. CONCLUSION

In order to have very low power consumption, we need to design devices which operate in subthreshold region. In this paper we have calculated the parameters of MOSFETs. The operation of CMOS Inverter in subthreshold region was simulated and comparison of Delays, Average Power and PDP are tabulated for 90 nm Technology in Cadence. From this the delay of CMOS Inverter is more in subthreshold region and power consumption is less compared to strong inversion region. The width of PMOS is varied up to 15u for an inverter to be operated in subthreshold region. By observing the power delay component operated in subthreshold region, supply voltage of 0.12 V is preferable for subthreshold operation.

6. REFERENCES

[1] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," Proceedings of the IEEE, vol. 91, no. 2, Feb. 2003

[2] A. Wang, B. H. Calhoun and A. Chandrakasan, Sub-threshold design for ultra low-power systems, Springer publishers, 2005

[3] C. H. Kim, H. Soeleman, and K. Roy, "Ultra-Low-Power DLMS Adaptive Filter for Hearing Aid Applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 11, no. 4, pp. 716-730, Aug. 2003

[4] J. Rabaey, Low Power Design Essentials, Springer publications, 2009.

[5] J. Rabaey, Digital Integrated Circuit Design by Jan M. Rabaey, Anantha P. Chandrakasan, Borivoje Nikolić, Borivoje Nikolić, Pearson Education, 2003

[6] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low- power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp. 473–484, Apr. 1992

[7] A. P. Chandrakasan and R.W. Brodersen, "Minimizing power consumption in digital CMOS circuits," Proc. IEEE, vol. 83, pp. 498–523, Apr. 1995.

[8] S. Kang, "Elements of Low Power Design for Integrated Systems," ISLPED '03, August, 2003.

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