AREA EFFICIENT RAPID SIGNAL ACQUISITIONSCHEME FOR HIGH DOPPLER DSSS SIGNALS

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ABSTRACT

The Direct Sequence Spread Spectrum (DSSS) communication system is widely used in ground to air missile links due to its anti-jam and low Signal to Noise Ratio (SNR) requirement advantages. The paper presents the challenges in achieving fast signal acquisition in this scenario and brings out the implementation challenges for achieving simultaneous Doppler estimation and phase delay of Pseudo Noise (PN) code. A new scheme for PN code phase delay estimation with correlation of differential signals, followed by precise Doppler estimation using Fast Fourier Transform (FFT) is presented. The area optimized Field Programmable Gate Array (FPGA) friendly architecture is utilized for rapid signal acquisition by combining both time and frequency domain approaches. The advanced design practices in FPGAs are used to achieve resource sharing and high clock speed of operation. The architecture is synthesized for Virtex-6 LX240T FPGA, resulting in 52% of area occupancy and 134 MHz of maximum allowed clock frequency value.

KEYWORDS

DSSS, signal acquisition, PN sequence, Doppler shift, carrier synchronization, PN code locking, GPS acquisition.

1.INTRODUCTION

The typical short range missile's guidance system consists of onboard communication equipment for receiving the guidance from control center. Usually the control center has some surveillance system (either RADAR or passive) by which the target is tracked at high rate. The communication link between the central guidance station and the missile is very crucial and must be designed to work in harsh environments. The DSSS communication system being highly robust for noise and jam proof, it is preferred in ground to air missile communication links. The paper [8] presents major issues in realizing the communication link between missile and control center and provides information on various spread spectrum schemes useful for this application. In such environments the link is likely to get disconnected several times during total flight time of missile. Hence the system must be able to reestablish the link within less time. Whenever link gets disconnected, the carrier and PN code synchronization must take place again. This is a

challenge to be achieved with high speed signal processing hardware. Majority of the DSSS signal acquisition architectures are built for GPS applications, where low cost hardware is main goal but not the high speed signal acquisition.

As in the described application it requires fast signal acquisition, there is a need for high speed dedicated hardware solution to achieve the same. Most of the existing designs evolved for GPS receiver applications use serial, parallel or semi-parallel techniques for signal acquisition. The conventional serial signal acquisition architecture is comparatively slow and occupies less silicon area. The parallel architectures employ FFT and multiply-accumulate blocks [1] at the expense of higher hardware cost. The work presented at [11] uses two levels of FFT to optimize on area, instead of using one single higher length FFT block. In this the first FFT layer was used for quick acquisition of code and carrier to give a coarse carrier frequency and second FFT layer was used for accurate frequency calculation based on the result of the first FFT layer. An acquisition method for GPS signals based on modified FFT is presented at [14]. The method uses Winograd Fourier transform algorithm (WFTA), prime factor FFT algorithm (PFA) and Cooley-Tukey FFT algorithm to perform FFT on the GPS IF signal samples. The technique proposed in this paper is to decompose large number point FFT into small number point FFTs. The work presented at [15] uses two channel based correlation and FFT for fast signal acquisition. The architecture attempts to increase the detecting probability, and solve the problem of acquisition at low carrier to noise ratio, in long PN code DSSS systems.

In addition to the problem of fast signal acquisition several researchers investigated on various other problems to improve the total reliability of DSSS systems. In paper [12] the problem of code acquisition for band-limited DSSS systems, in the presence of sampling offset is studied. An improved acquisition scheme is presented which utilizes two decision variables (with and without the existence of sampling offset) for joint noncoherent detection. The work presented at [13] explains the usage of compressive sensing in spread spectrum systems to achieve energy efficient hardware architecture. The usage of compressive sensing based algorithms for DSSS signal acquisition requires a closer look, as it allows to work with higher bandwidth signals for given clock frequency limitations of hardware.

The DSSS signal acquisition module for proposed application scenario has more strict timing requirements in comparison with typical GPS signal acquisition techniques found in literature. The standard GPS signal has the navigation data changing at 50 Hz, which corresponds to 20 ms time period for information bit. Hence even the fastest signal acquisition techniques used in real time GPS receivers are less complex in comparison with DSSS link aimed for missile guidance system. In the proposed context the bit rate can even go up to few tens of Kbps, where as in GPS it is only 50 Hz. Another factor which makes the signal acquisition more complicated is the acquisition code length without any phase changes in between. In case of GPS the Gold code length is 1023 chips and chip rate is 1.023 MHz, which completes one PN sequence in 1 millisecond. Higher integration time is available since one navigation bit is 20 ms and covers 20 Gold code sequences continuously with no phase shift. Hence signal detection is possible even with low SNR conditions. Usually in GPS 10 ms of acquisition time in a window of 20 ms is used such that 10 Gold code sequences can be integrated without any phase change [1] due to navigation bits. In the given requirement of DSSS link system it is not possible as navigation data comes at high rate and so each navigation bit can only have one or two Gold code sequence in it. So the acquisition has to perform with one Gold code sequence only. In case of GPS the typically considered Doppler is 10 KHz, where as in the missile to control center link case Doppler can shift the carrier in a band of 60 KHz. This makes the design more challenging towards achieving

lower acquisition time. To achieve rapid signal acquisition, complete FPGA solution is required. On FPGA platform it is possible to do acquisition and tracking using different parameters and threshold values which give total flexibility of operation to the user. This implementation style also helps in up- gradation of logic for any future requirements catering for various PN code sizes and Doppler shifts.

2.PROPOSED ARCHITECTURE

In this section the step by step derivation of proposed architecture from the existing architectures is explained. The proposed scheme utilizes time domain correlation for PN code phase acquisition and frequency domain Doppler acquisition. The problem of signal acquisition can be visualized as simultaneous estimation of phase of PN code and Doppler shift. The figure 1, illustrates this requirement as a two dimensional (2D) search.

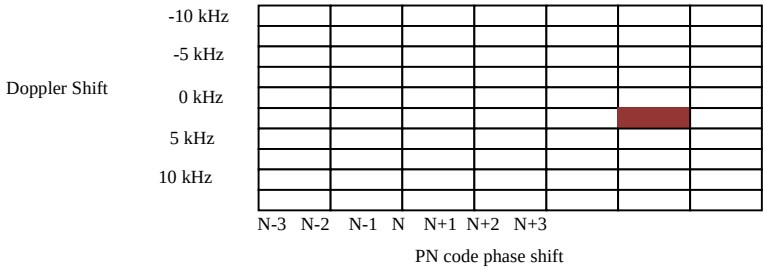

Figure 1 PN code phase delay and Doppler estimations

The serial and parallel FFT based architectures of simultaneous PN code acquisition and Doppler estimation, are well discussed in [2][9][10]. Usually Field Programmable Gate Arrays (FPGAs) are used to realize the high speed acquisition algorithms. The serial acquisitions suffer from long acquisition delays and hence do not meet the requirements of described application context, where as parallel has higher implementation cost. It is to be noted that in parallel architectures as the PN code length increases, the implementation cost (FPGA area occupancy) grows exponentially. Hence the parallel architectures in direct form cannot be implemented in practical FPGA hardware for long PN code based DSSS systems.

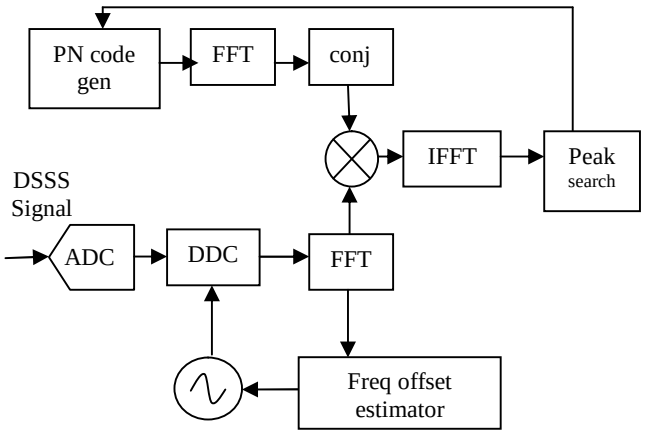

Figure 2. Typical FFT based acquisition – high level block diagram

In the proposed architectures so far, appreciable frequency resolution for estimating the Doppler is required to ensure the correct PN code phase delay estimation. To achieve this, the FFT size must be high and hence it results in higher implementation cost. The high level block diagram of such technique is given in figure 2. Several variants of this architecture are well discussed in literature [1][3][5][6][7]. The basic principle is to find the cross spectral density and hence to estimate the PN code phase offset between signal being acquired and locally generated PN code. The Doppler frequency estimation and correction loop ensures the carrier tracking. Another drawback of majority of FFT based schemes are that they require FFT implementation which is not power of 2. Such algorithms cannot use the features of FPGA vendor provided FFT libraries. The schemes presented so far cannot estimate the PN code phase shift without a reasonably good estimate of the carrier. Hence the computational effort while searching in 2D search space is more. The scheme presented in this paper can make the estimation of PN code phase shift even in the case when the Doppler estimation is not completed.

a.Effect of low frequency carrier/Doppler residue

It is evident from the basic principle that during the first few iterations of the acquisition, there is a mismatch between the incoming signal's carrier frequency and local generated carrier. This results in low frequency envelope over the DSSS signal. The figure 3 depicts this scenario in high SNR conditions for clear understanding of the issue. The high frequency chips of DSSS PN code are modulated with low frequency carrier residue.

Figure 3. Effect of low frequency carrier residue on received PN code.

The time domain received signal at IF level can be described as below.

$$x_1(t) = K_1.c(t).d(t).\cos[(\omega_{IF} + \omega_d).t + \theta] + n(t) \quad (1)$$

The chip bits are represented with c(t) and data bits are represented with d(t). The DSSS carrier is considered to be available at ω_{IF} angular frequency and ω_d is the angular frequency resulting with Doppler shift. The term θ is the random phase mismatch between DSSS transmitter and receiver. Overall attenuation/gain factor is considered as K1. The additive white Gaussian noise $n(t)$ is considered to be uncorrelated with signal and is generated from another statistically independent source.

Considering the Digital Down Converter (DDC) tuning frequency as $\omega_{IF}+\omega_o$, the DDC output $x_2(t)$ shall consist the frequency terms: $\omega_d + \omega_o$ and $\omega_d - \omega_o$. Whereas ω_o is the frequency mismatch between local oscillators of both transmitter and receiver. Note that other high frequency terms are filtered by DDC filter. These low frequency terms result as envelope on DSSS signal as shown in figure 3. In figure 3, high SNR condition is taken for better visual understanding of the situation.

b. Time domain correlator on differential signals

With the presence of The Doppler shift and carrier frequency mismatch, the low frequency envelope present on the DSSS signal causes poor correlation peak in the DSSS correlator. The effect of negative and positive excursions of envelope results in inversion of spread code in it. This results in reduced correlation peak. However it can be shown that the transitions of chips are only weighted by the instantaneous envelope value, preserving the phase transition information of PN code both in positive and negative excursions of envelope. Based on this property, correlation is performed on differential versions of both local generated PN code and received signal. The Circular Cross Correlation (CCC) is used to estimate the correlation peak.

$$Y_{corr} = CCC\left(x_{1d}(t), C_{rd}(t)\right) \quad (2)$$

The $x_{1d}(t)$ and $C_{rd}(t)$are the first order differential signals of $x_1(t)$ and $C_r(t)$ respectively. The $C_r(t)$ is the receiver side local generated PN code. The receiver architecture based on this principle and its simulation results are explained in further sections.

c. Specifications

The specifications considered for design are listed out in table 1.

TABLE I. Specifications considered for design

	Specifications		
	Parameter	Value	comments
1	Informationi bit rate	2.5 kbps	Minimum missile command link requirements[8]
2	PN code length	1023	Gold code
3	Number of PN code sequences per data bit	2	Note that this is 20 in case of GPS
4	Chip rate	5.115 Mbps	
5	Modulation type	BPSK	
6	IF frequency	25.575 MHz	Selected 1/4th of Fs to optimize the NCO design in DDC
7	Sampling frequency	102.3 MHz	
8	Decimation factor in DDC	4	
9	DDC filter taps	64	Polyphase decimation filter
10	Doppler shift	±20 kHz	
11	Frequency mismatch in Tx and Rx	±10 kHz	
12	Spectrum estimation FFT size	32768	Achieved resolution 780Hz in Doppler estimation
13	SNR	5 dB	

The specifications are selected to result in area optimized implementations of DDC to achieve multiplications by only {+1, 0,-1, 0} in the Numerically Controlled Oscillator (NCO) multiplication stage. This also ensures no bit growth at the NCO multiplication stage.

d. High level block diagram

The complete DSSS system is simulated both in MATLAB and VHDL consisting of the blocks shown in figure 4. The complete system is simulated at the IF level. The baseband data generator module generates test data for the entire system. The 1023 length Gold code generator is used for spreading the information bits. One information bit is spread with two PN sequences resulting in 5.115 Mbps chip rate. The BPSK modulator produces DSSS signal at the selected IF frequency. In typical SDR implementation of DSSS transmitter, a DAC stage followed by up-converter generates the DSSS signal at the frequency of interest. On the receiver side the DSSS signal is converted to the required IF frequency band of interest by the front end RF system. These blocks are not modeled in current simulation. However an AWGN simulator is used to introduce the noise to bring the signal to 5 dB SNR.

The ADC samples the signal at 102.3 Msps rate. The output of ADC is of signed numbers represented in 2's complement binary. An 8-bit ADC is considered in the present simulation which is valid for DSSS based systems. This block also consists of necessary clocking and synchronizing circuitry required for ADC. The front end Digital Down Converter (DDC) turns the IF band level signal to base band. In achieving this, Numerically Controlled Oscillator (NCO) is tuned to the initial carrier frequency value. Here the IF frequency and hence the NCO output frequency is selected to be 1/4th of sampling frequency. This avoids need of block RAMs in FPGA for realizing NCO. This also allows the realization of NCO multiplication stage in area optimized way by only multiplying with {+1, 0,-1, 0} for COS and {0,-1, 0, +1} for negative SIN respectively. The NCO multiplication is the only stage where the logic need to run at Fs and all further stages runs with decimated clock Fsd. The choice of Fo = Fs / 4, also ensures that higher sampling rates are supported on given FPGA technology.

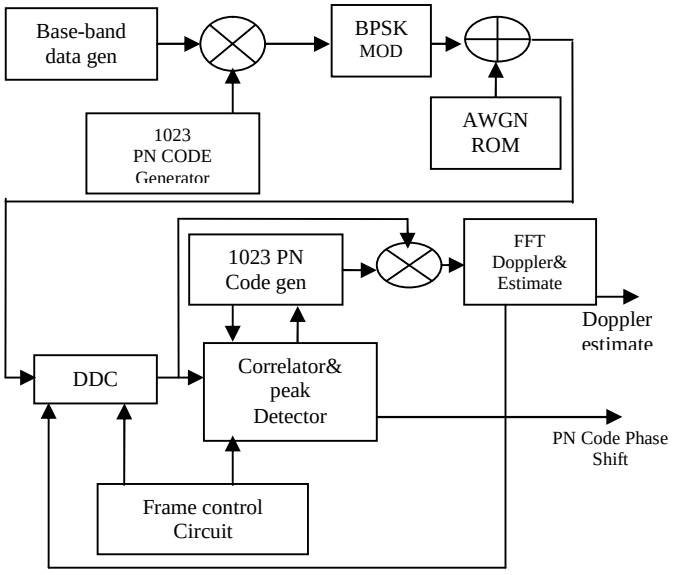

Figure 4. High level block diagram of simulated DSSS system

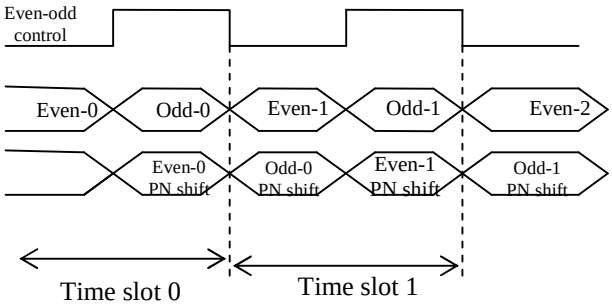

Figure 5. Pipelined processing of consecutive frames

The PN code phase delay estimation is computed in pipelined architecture with each time slot consisting two frames. The time slot interval is equal to information bit period. As there are two PN code lengths in each bit interval, we must estimate the PN code phase shift in two consecutive frames and detect the maximum peak. The frame with maximum CCC peak corresponds to the time duration over which there is no bit change in base band information data. This approach can be compared with selecting one among two 10 ms time slots for GPS acquisition [1]. As shown in figure 5, the peak estimation on CCC takes place in next frame interval. This ensures that local PN code is circularly rotated by the estimated phase shift by the next correlation cycle. This high speed architecture allows the PN code phase estimation by the end of first time slot and aligns the PN code phase by next time slot. So practically it is possible to achieve the PN code synchronization within 2 time slots. In the current implementation, this corresponds to 0.4 ms.

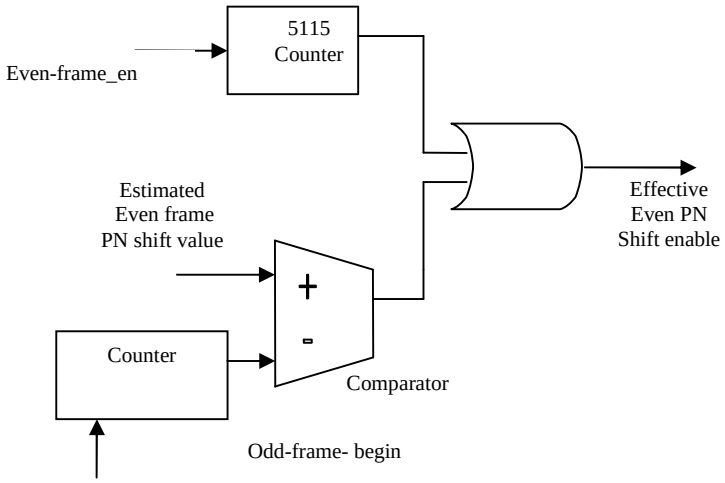

Figure 6. Circuit shift enable for differential PN code of EVEN frame

The CCC operation consumes large DSP48 slices in FPGA hardware if it is implemented in conventional manner. Note that each PN code length is over sampled by 5, hence total stream of 5115 samples corresponds to one PN code sequence. The differential PN code is circular shifted and used for correlation along with the continuously obtained difference of the DDC output. Two copies of differential PN code are maintained corresponding both even frame and odd frame. The circuit shift enable generation logic for even frame is illustrated in figure 6. The CCC is

implemented in highly area efficient manner using serial in serial out (SISO) shift registers, multiplexers and accumulators as shown in figure 7.

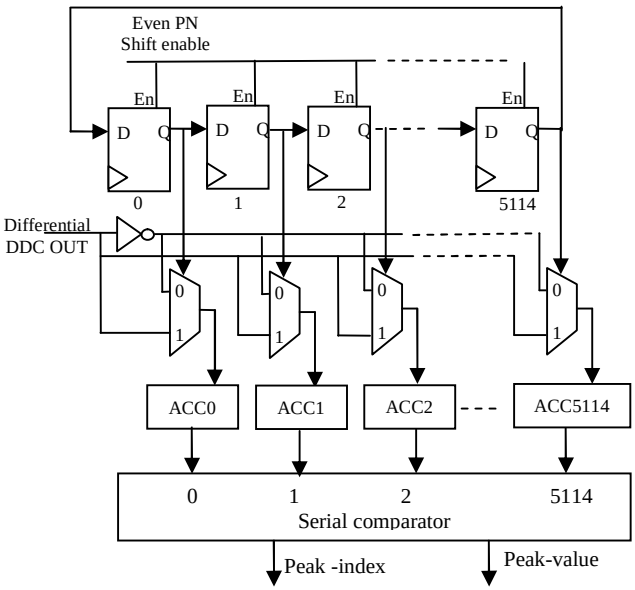

Figure 7. VHDL implemented Area efficient time domain CCC

While computing the CCC for even frame the rotation for continuous 5115 clock cycles is required. During the odd-0 frame correlation time, first the peak estimation among the even-0 frame's CCC output is computed and subsequently enable signal is generated for rotating the even frame's differential PN code. To run this logic at high speed this section of logic made to run at 102.3 MHz instead of 25.575 MHz. This ensures the phase shifted differential PN code is available by even-1 correlation time.

The chain of 5115 number of DFFs connected in SISO shift register style are used for circular shifting the differential PN code signal. The series of multiplexers are used to realize the multiplication of differential DDC output signal with differential PN code. The series of accumulators integrate the product terms corresponding to the CCC coefficients for all phase shifts. The serial comparator estimates the maximum value and index. Same hardware block is used for even frame and odd frame. Only final set of latches are different to hold the correlation peak index and correlation peak value. The phase estimated from this CCC block is used to shift the PN code (not the differential PN code) and multiply with the DDC output. This product should ideally generate CW signal of frequency equal to Doppler shift and other frequency offsets. This signal is given to 32K FFT block as shown in figure 4, for frequency estimation. This frequency value shall be utilized to tune the analog PLL in mixer stage to correct the carrier to exact IF value. Note that the choice of digital correction can also be used at the expense of replacing the area optimized NCO with complete direct digital synthesis (DDS) core followed by I and Q multipliers. In that case the digital correction of NCO frequency can be achieved by changing the phase increment word.

3. SIMULATION RESULTS

a. MATLAB simulation results

The concept of differential signal's correlation for efficient PN code shift estimation is initially simulated in MATLAB and proof of concept is established.

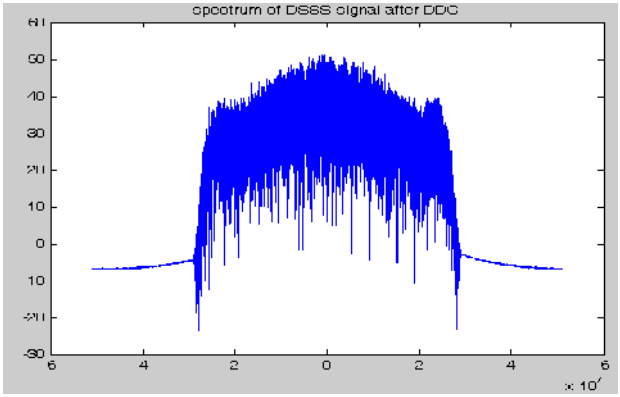

Figure 8. Spectrum of DSSS signal at the DDC output

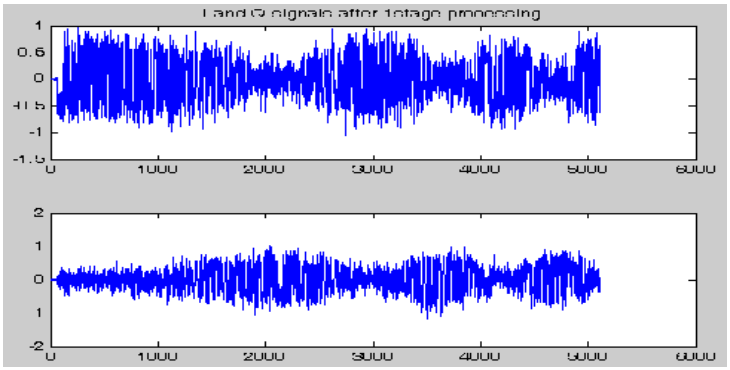

Figure 9. I and Q at DDC output (envelope due to Doppler)

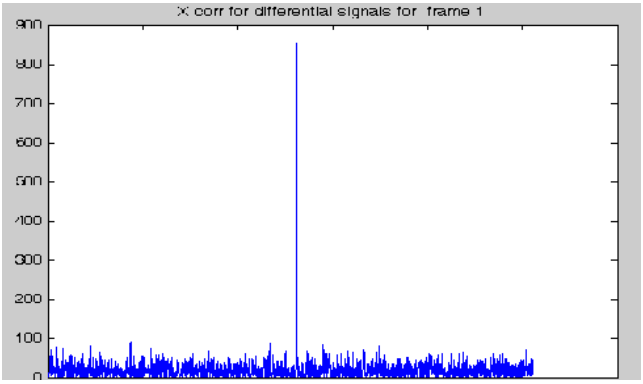

Figure 10. CCC peak for differential input signals

The figure 8 to 10 shows the obtained MATLAB simulation results. The figure 9 shows the DDC output in time domain whose difference is used for computing the CCC. The peak of CCC function is shown in figure 10. The peak indicates the PN code phase shift required for achieving synchronization.

As the logic is aimed for FPGA hardware realization, VHDL simulation is also carried out and results are validated. The block sizes of 32K complex samples are used in every iteration while estimating the Doppler shift. The frequency correction accuracy and correction time intervals for these parameters are estimated below.

sampling rate after decimation $F_{SD} = \frac{F_S}{D}$

$$F_{SD} = 25.575 \text{ MHz}$$
$$T_{SD} = 39.10 \text{ nsec}$$

$$\text{Frequency resolution} = \frac{F_{SD}}{N_{FFT}} = 780 \text{ Hz}$$

$$\text{Time reuquired to process one block } T_B = N_{FFT} \cdot T_{SD}$$
$$T_B = 1.28 \text{ msec}$$

Hence with the proposed architecture the correction of frequency and phase offset in PN code is carried out at every 1.28 m sec and 0.4 m sec interval respectively. The architecture wise achieved frequency correction accuracy is 780 Hz and phase correction accuracy is 1/5th of chip interval. These parameters are sufficient for the targeted applications.

b.VHDL simulation results

The VHDL simulation for the implemented DSSS communication system as given in figure 4, is carried out using Modelsim simulation tool. The Obtained VHDL simulation results are shown in figure 11 to 14.

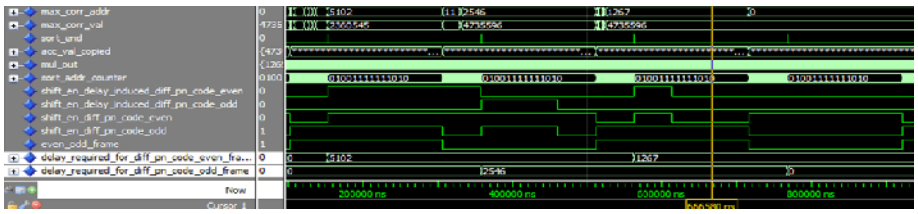

Figure 11. VHDL simulation results showing even odd frame related control signals and shift enable signals

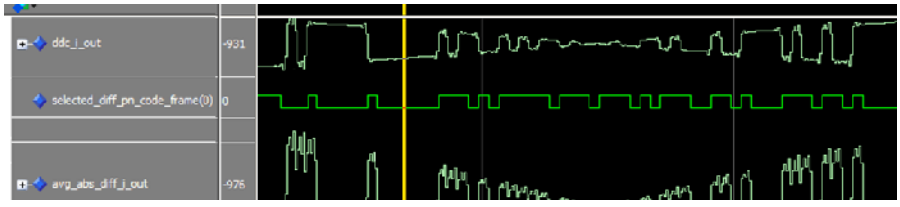

Figure 12. Results showing the DDC out(first), differential PN code(second) and differential DDC out(third)

The results are validated minimum at 5 dB SNR. As the waveforms are difficult to interpret visually to derive conclusions at 5 dB SNR, the results are shown here at 30 dB SNR. The figure 11, shows the shift enable signals for even and odd frames. The signal even_odd_frame indicates the current frame type. In case of '0' it is even frame and in case of '1' it is odd frame.

The figure 12, shows the differential PN code and differential DDC out. It can be noticed that even after zero crossing of low frequency envelope both the differential signals maintain coherency. This is the key for proposed technique to achieve correct PN shift even the Doppler is not estimated from the signal. The assumption of chip rate being much higher than the low frequency envelope is valid in any DSSS system.

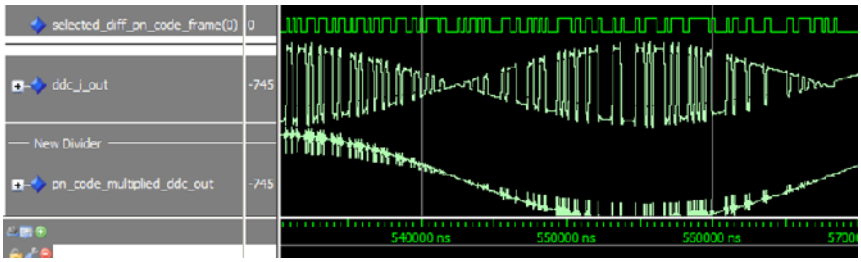

Figure 13. Results showing PN code (first), DDC out(second) and their product (third)

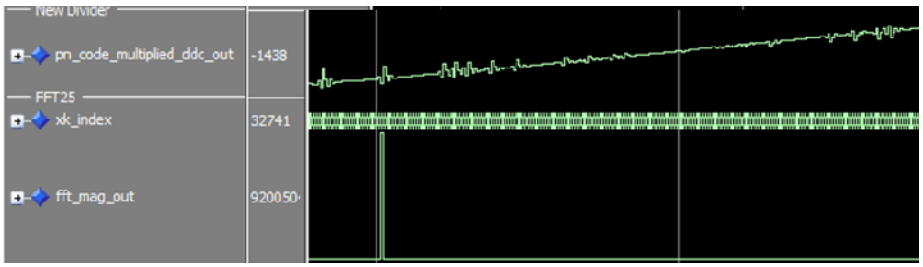

Figure 14. Results showing DDC out & PN code product (first), FFT out index (second) and FFT out magnitude (third)

Figure 13, shows the resulting carrier after the multiplication of DDC output and phase adjusted PN code. This signal is applied to FFT block to estimate the frequency of Doppler as shown in figure 14. The peak showing at 32741indicates the offset of 27 bins from zero, which is result due to 20 KHz Doppler introduced.

c.FPGA Synthsis

The simulation level verified VHDL code is synthesized using Xilinx ISE 12.3 tool. The Virtex-6 FPGA LX240T is selected for the synthesis and performance estimate. The complete DSSS system, even with modules of transmitter and AWGN along with receiver occupies 52% of area and 134 MHz of maximum frequency of operation.

CONCLUSIONS

The work presents rapid signal acquisition scheme which can acquire the DSSS signal with pipelined PN code phase shift estimation logic, using CCC of differential signals. Architecture is developed such that it can track the signal even under frequency residue up to 30 K Hz. The scheme finds application in developing missile communication links with DSSS modulation. The estimated area occupancy and speed with Xilinx ISE show that the scheme can be implemented in FPGA hardware. Several blocks are redesigned to give area optimized implementation to ensure the scalability of the code for higher PN code lengths and higher Doppler shifts. The work aimed to be continued in FPGA implementation and testing on hardware.

ACKNOWLEDGMENT

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REFERENCES

[1] JAMESBAO-YENTSUI, "Fundamentals of Global Positioning System Receivers A Software Approach", second edition, AJOHNWILEY&SONS,INC.,PUBLICATION

[2] Dinesh MANANDHAR Yongcheol SUH and Ryosuke SHIBASAKI "GPS Signal Acquisition and Tracking An Approach towards Development of Software-based GPS Receiver"

[3] Falin Wu, Kefei Zhang and Akio Yasuda, "GPS signal acqiusition and tracking using software GPS receiver", The Eighth International Symposium on Signal Processing and its Applications, IEEE 2005. Vol-2, 843-846

[4] Abdulqadir Alaqeeli, Janusz Starzvk and Frank van Graas, "Real time acquisition and tracking for GPS recivers", IEEE Interntional symposium on circuits and systems – ISCAS 2003,V-4 , 500-503

[5] Jing Pang, Janusz Starzyk, "Fast Direct GPS Signal Acquisition Using FPGA", School of Electrical Engineering and Computer Science, Ohio University, Athens

[6] ZhenZhu, FrankvanGraas, JanuszStarzyk , "GPS signal acquisition using the repeatability of successive code phase measurements",

[7] Abdulqadir Alaqeeli and Janusz Starzyk, "Hardware Implementation for Fast Convolution with a PN Code Using Field Programmable Gate Array". Proceedings of the 33rd Southeastern Symposium on System theory, IEEE 2001, 197-201

[8] Atul Govindrao Pawar, "Wireless Communication in Missiles: Challenges", DRDO Science Spectrum, March 2009, pp. 230-235, DESIDOC

[9] Fernando D.Nunes and Jos´e M.N.Leit˜ao "A New Fast Code/Frequency Acquisition Algorithm for GPS C/A Signals", IEEE 58th Vehicular Technology Conference, 2003. VTC 2003, Vol 2, 766-770

[10] Geng Sheng-qun and WU-liang "An FFT based acquisition algorithm for spread spectrum signal in high dynamic" IEEE 2005 International conference on Communications, Circuits and Systems, Vol 2.

[11] Sun Guoliang, "A Fast Acquisition Method of DSSS Signal Based on Double FFT Layers" IEEE WRI World Congress on Computer Science and Information Engineering, 2009, 452-456

[12] Ding and Sheng, "An Improved Code Acquisition Scheme for Band-limited DSSS Systems with Sampling Offset", IEEE communication letters, August 2012, Vol 16 , Issue: 8 , 1169-1172.

[13] Karsten Fyhn, Thomas Arildsen, Torben Larsen and Søren Holdt Jensen, "Demodulating subsampled Direct Sequence Spread Spectrum signals using compressive signal processing" IEEE Proceedings of the 20th European Signal Processing Conference (EUSIPCO), 2012, 2556 - 2560.

[14] Chunyu Li and Jianfeng Guan, "Code acquisition method of GPS signals based on WFTA, PFA and Cooley-Tukey FFT" IEEE International Conference on Intelligent Control, Automatic Detection and High-End Equipment (ICADE) 2012, 119-122.

[15] Liu Suxiao, Feng Wenquan, Xiong Huagang, Wang Dong and Liu Xi, "A FFT based long-code acquisition algorithm suitable for FPGA implementation", IEEE International Conference on Electric Information and Control Engineering (ICEICE), 2011, 5621 - 5624